Fig. 1

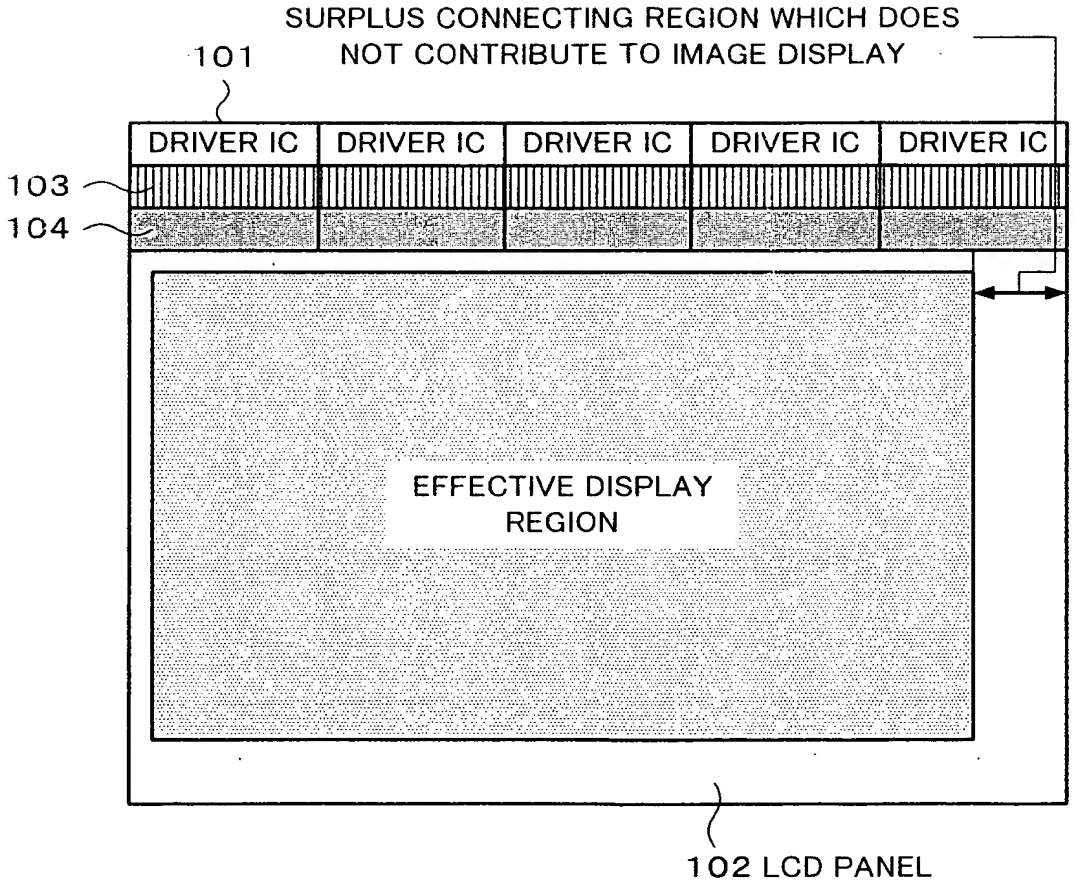

SURPLUS CONNECTING REGION WHICH DOES NOT CONTRIBUTE TO IMAGE DISPLAY
101
DRIVER IC
DRIVER IC
DRIVER IC
DRIVER IC
DRIVER IC
103
104
EFFECTIVE DISPLAY REGION
102 LCD PANEL

Fig. 2

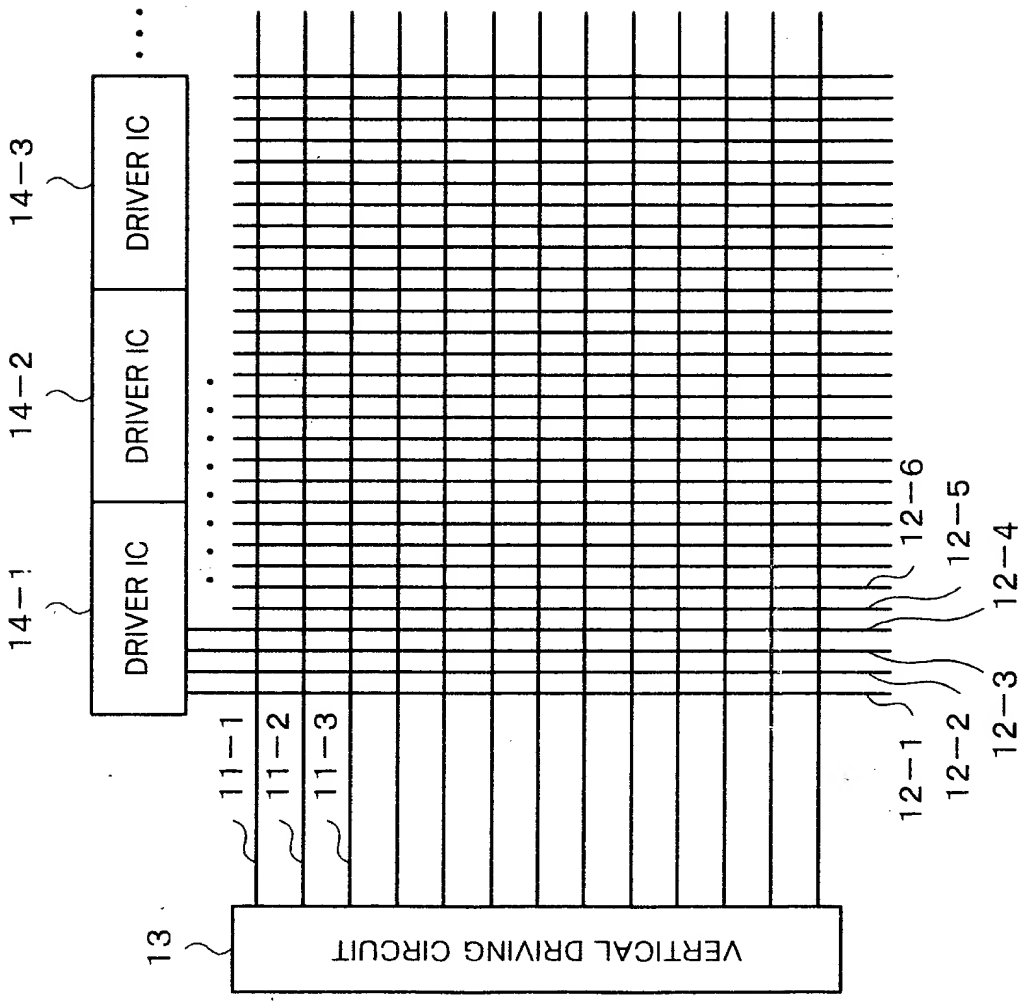

DRIVER IC
DRIVER IC
DRIVER IC
14-1
14-2
14-3
11-1
11-2
11-3
12-1
12-2
12-3
12-4
12-5
12-6
13
VERTICAL DRIVING CIRCUIT

Fig. 3

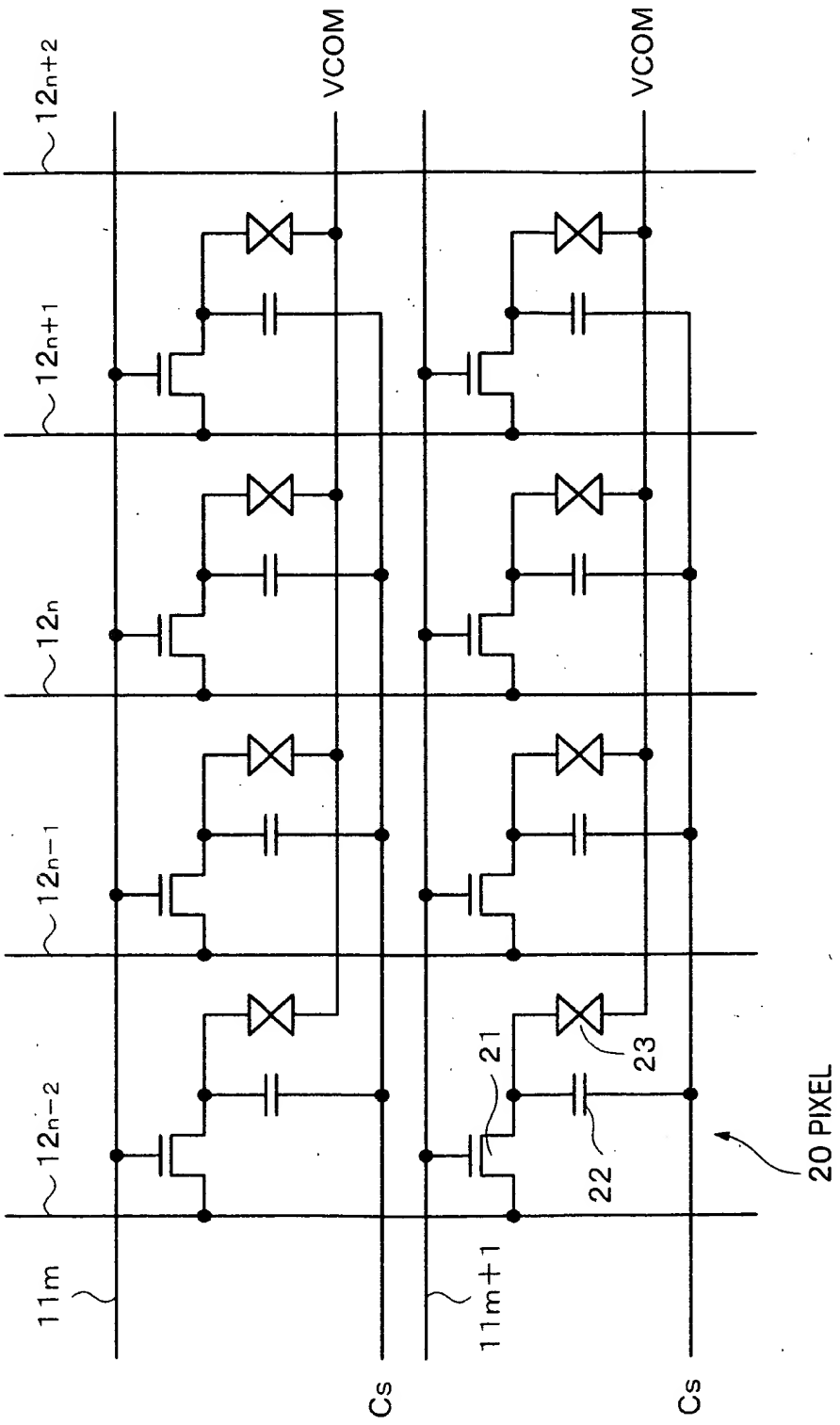

12n+2
12n+1
12n
12n-1
12n-2
11m
11m+1
VCOM
VCOM
Cs
Cs
21
22
23
20 PIXEL

Fig. 4

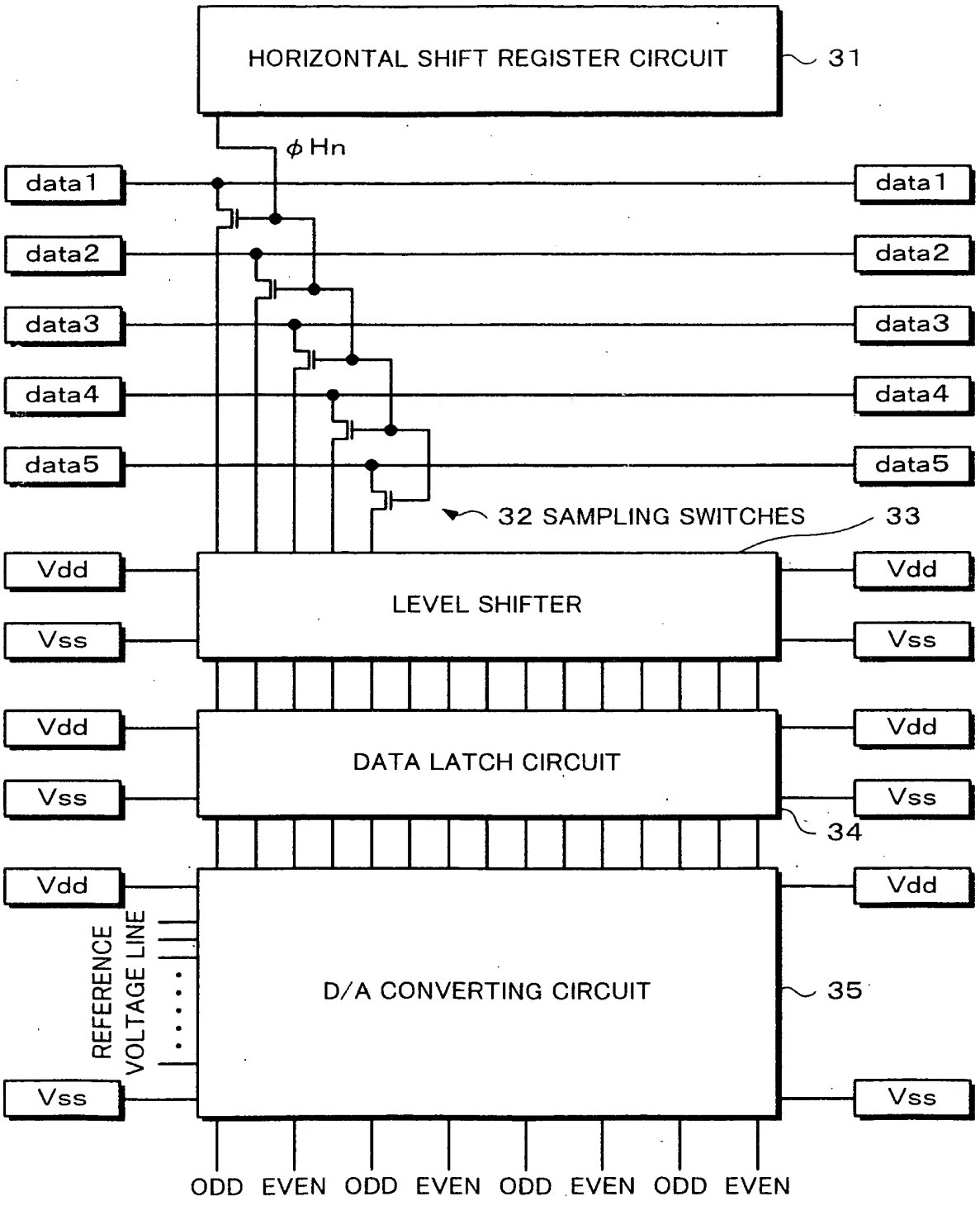

HORIZONTAL SHIFT REGISTER CIRCUIT
31
φHn
data1
data2
data3
data4
data5
32 SAMPLING SWITCHES
33
Vdd
Vss
LEVEL SHIFTER
DATA LATCH CIRCUIT
34
REFERENCE VOLTAGE LINE
D/A CONVERTING CIRCUIT
35
ODD EVEN ODD EVEN ODD EVEN ODD EVEN

Fig. 5

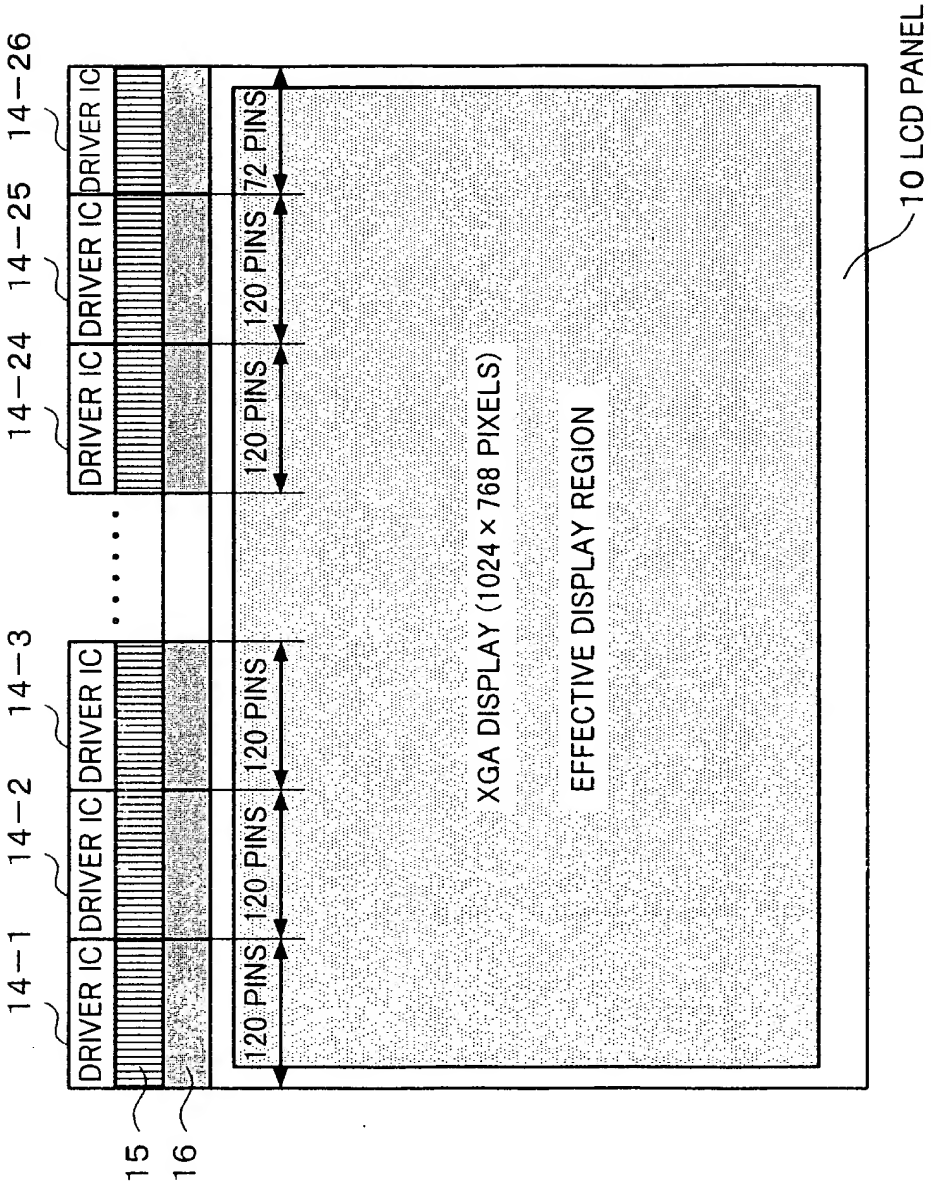

14-1
14-2
14-3
14-24
14-25
14-26
DRIVER IC
120 PINS
72 PINS
XGA DISPLAY (1024 × 768 PIXELS)
EFFECTIVE DISPLAY REGION
10 LCD PANEL
15
16

Fig. 6

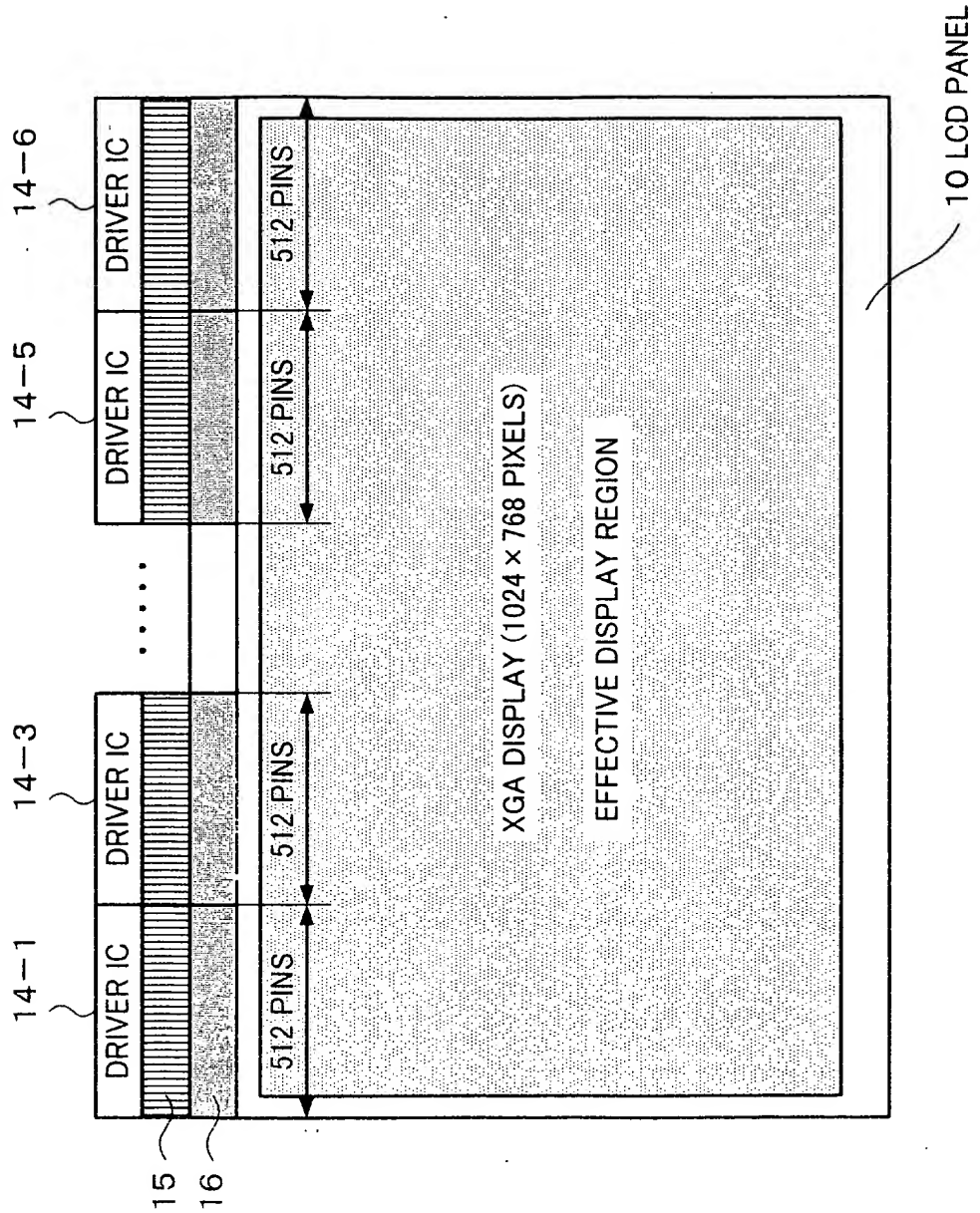

14-1
14-3
14-5
14-6
DRIVER IC
DRIVER IC
DRIVER IC
DRIVER IC
512 PINS
512 PINS
512 PINS
512 PINS
XGA DISPLAY (1024 × 768 PIXELS)
EFFECTIVE DISPLAY REGION
10 LCD PANEL
15
16

Fig. 7

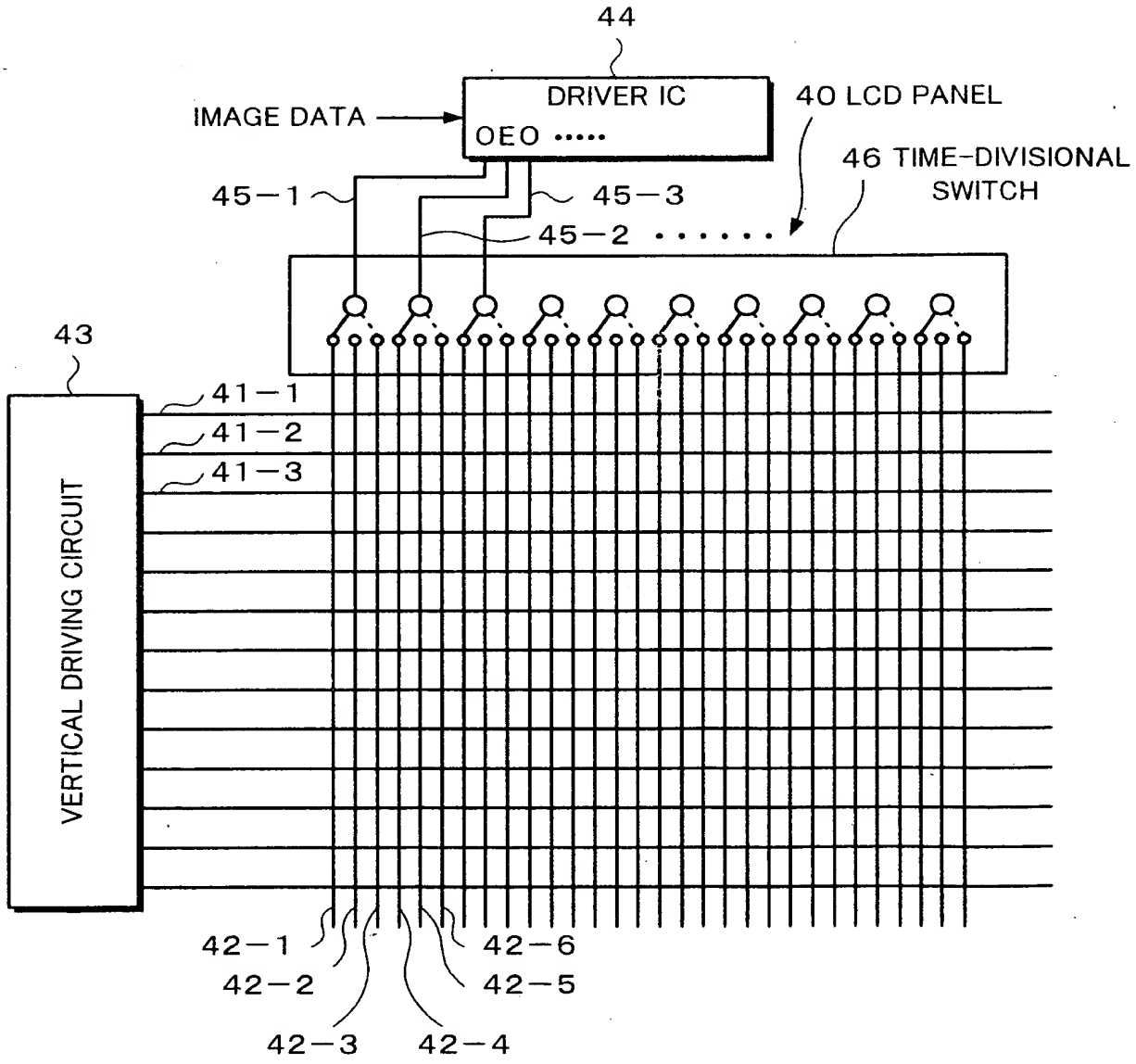

44
DRIVER IC
OEO .....
IMAGE DATA
40 LCD PANEL
46 TIME-DIVISIONAL SWITCH
45−1
45−3
45−2 .....
43
VERTICAL DRIVING CIRCUIT
41−1
41−2
41−3
42−1
42−2
42−3
42−4
42−5
42−6

Fig. 8

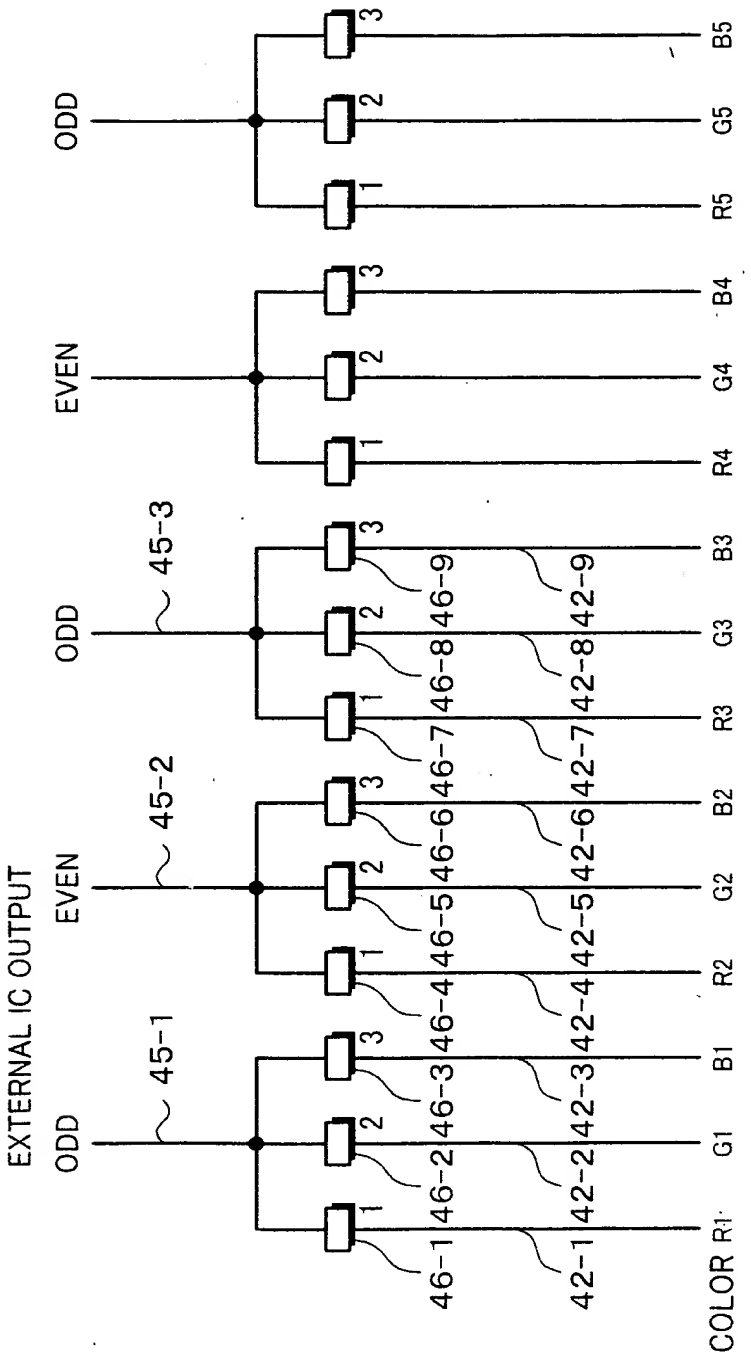

EXTERNAL IC OUTPUT
ODD
EVEN
ODD
EVEN
ODD
45-1
45-2
45-3
1
2
3
46-1
46-2
46-3
46-4
46-5
46-6
46-7
46-8
46-9
42-1
42-2
42-3
42-4
42-5
42-6
42-7
42-8
42-9
COLOR R1
G1
B1
R2
G2
B2
R3
G3
B3
R4
G4
B4
R5
G5
B5

Fig. 9

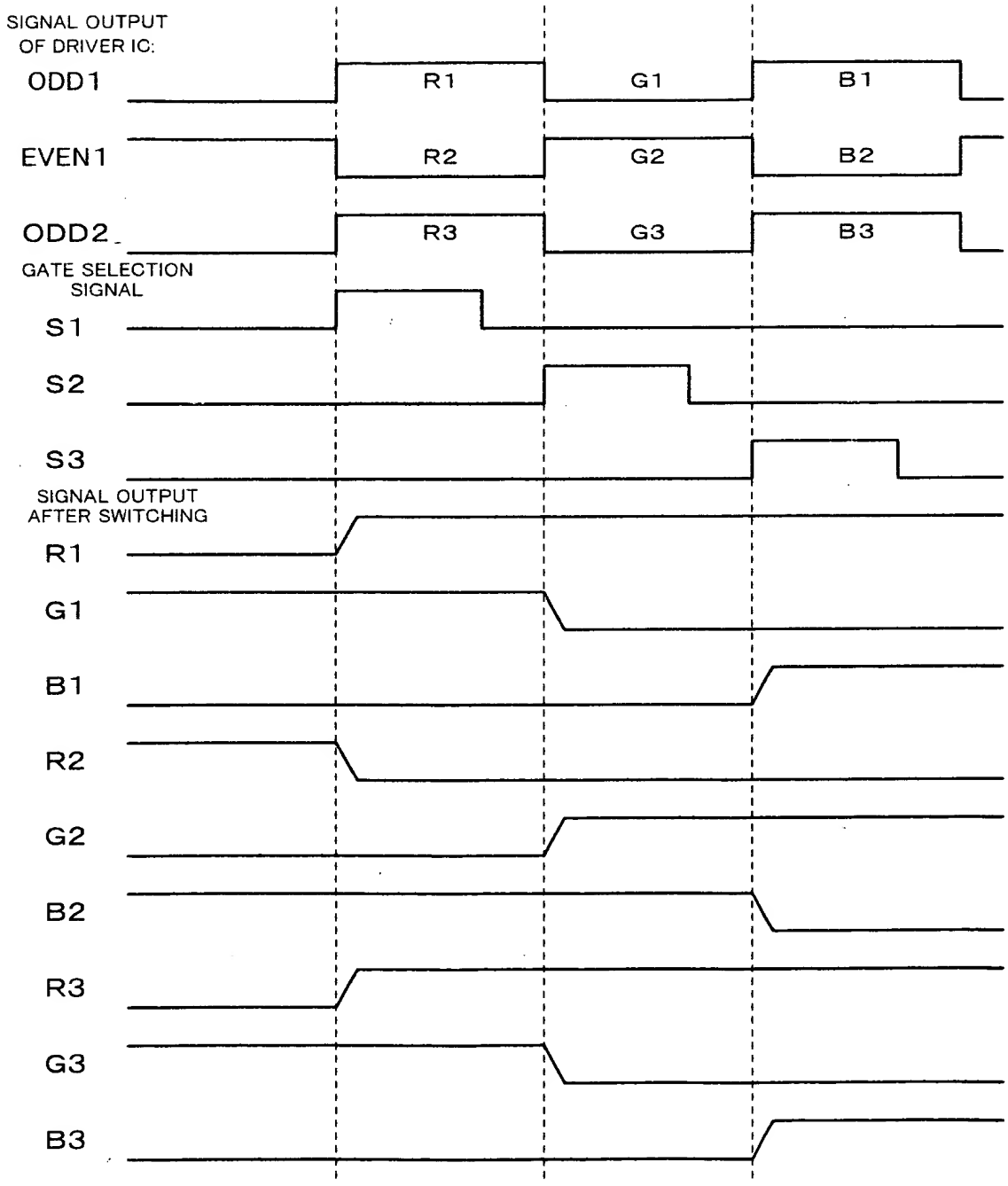

SIGNAL OUTPUT OF DRIVER IC:
ODD1
R1
G1
B1
EVEN1
R2
G2
B2
ODD2
R3
G3
B3
GATE SELECTION SIGNAL
S1
S2
S3
SIGNAL OUTPUT AFTER SWITCHING
R1
G1
B1
R2
G2
B2
R3
G3
B3

Fig. 10

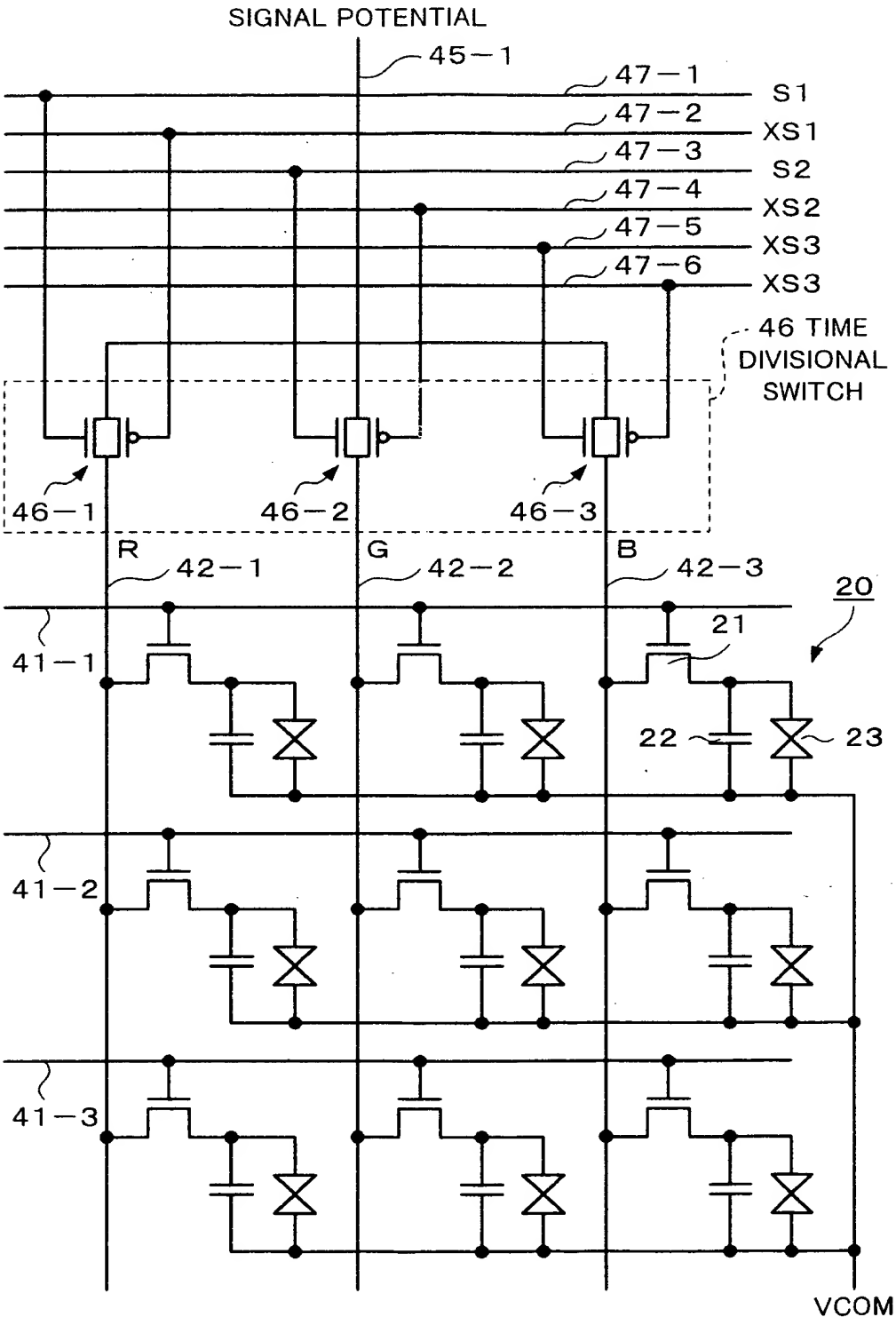

SIGNAL POTENTIAL
45−1
47−1
S1
47−2
XS1
47−3
S2
47−4
XS2
47−5
XS3
47−6
XS3
46 TIME DIVISIONAL SWITCH
46−1
46−2
46−3
R
G
B
42−1
42−2
42−3
20
21
22
23
41−1
41−2
41−3
VCOM

Fig. 11A

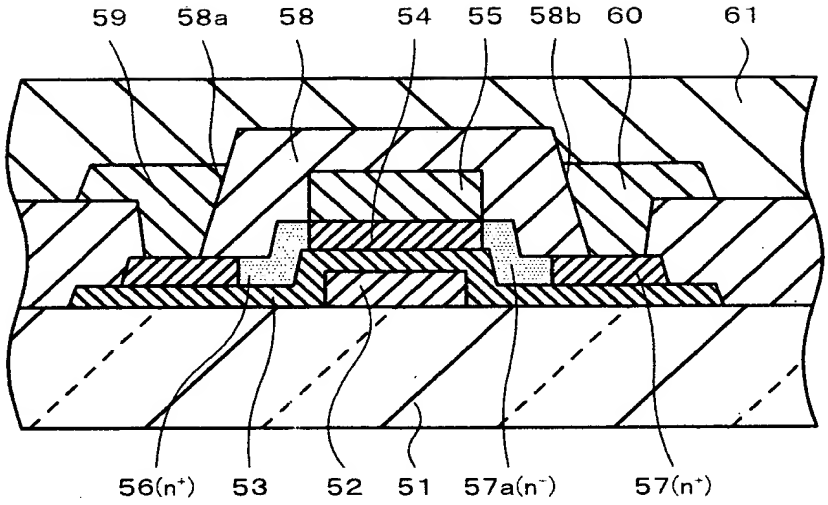


Fig. 11B

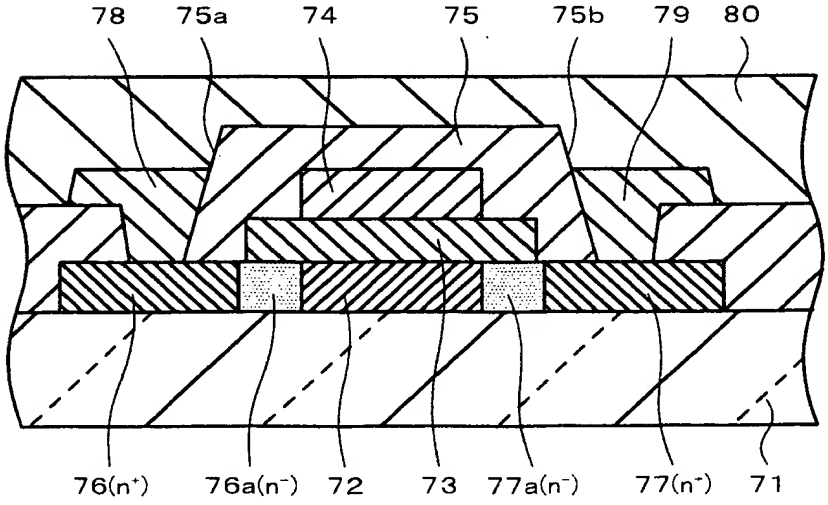


Fig. 12

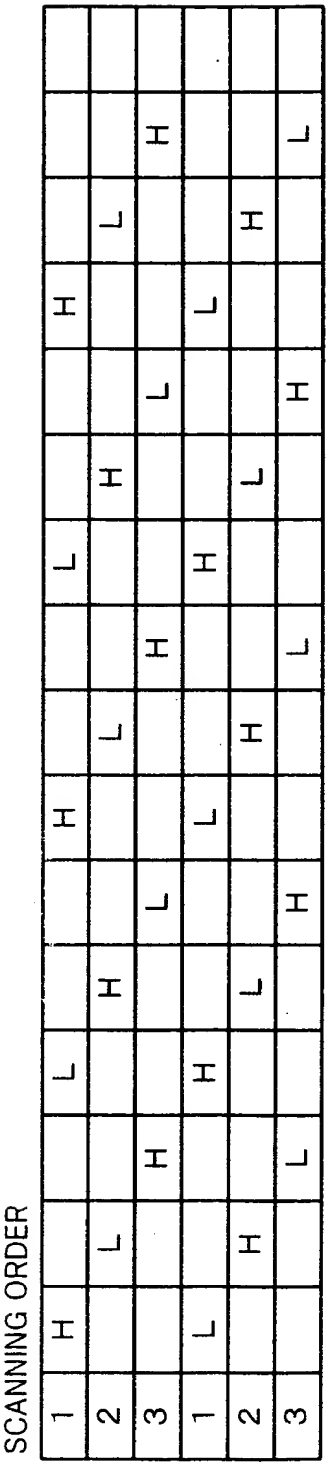


Fig. 13A

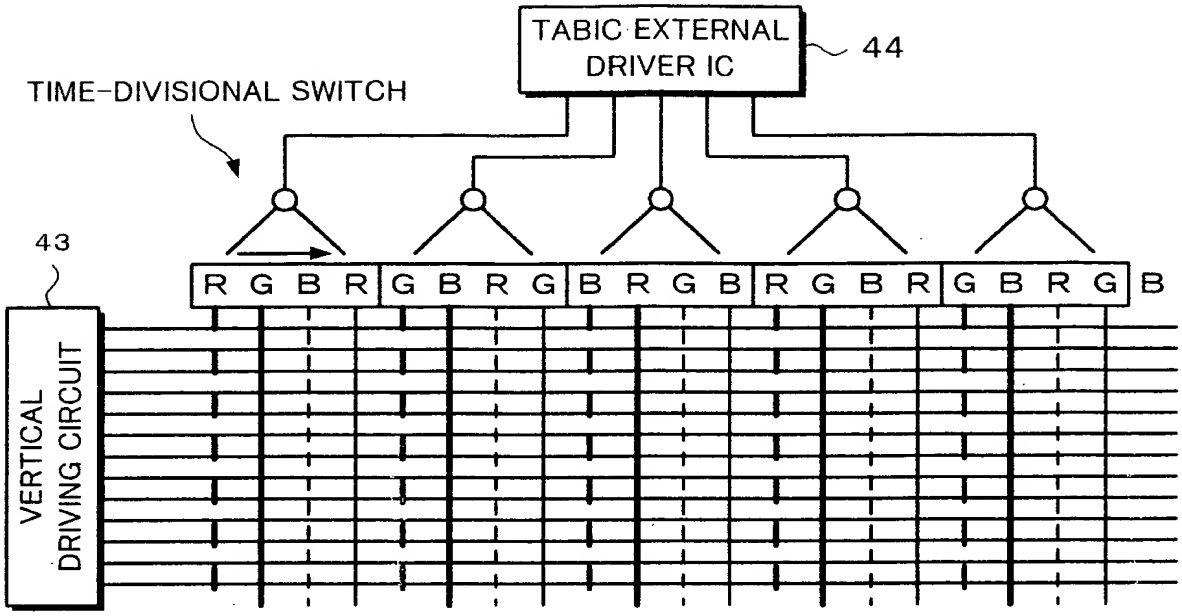


Fig. 13B

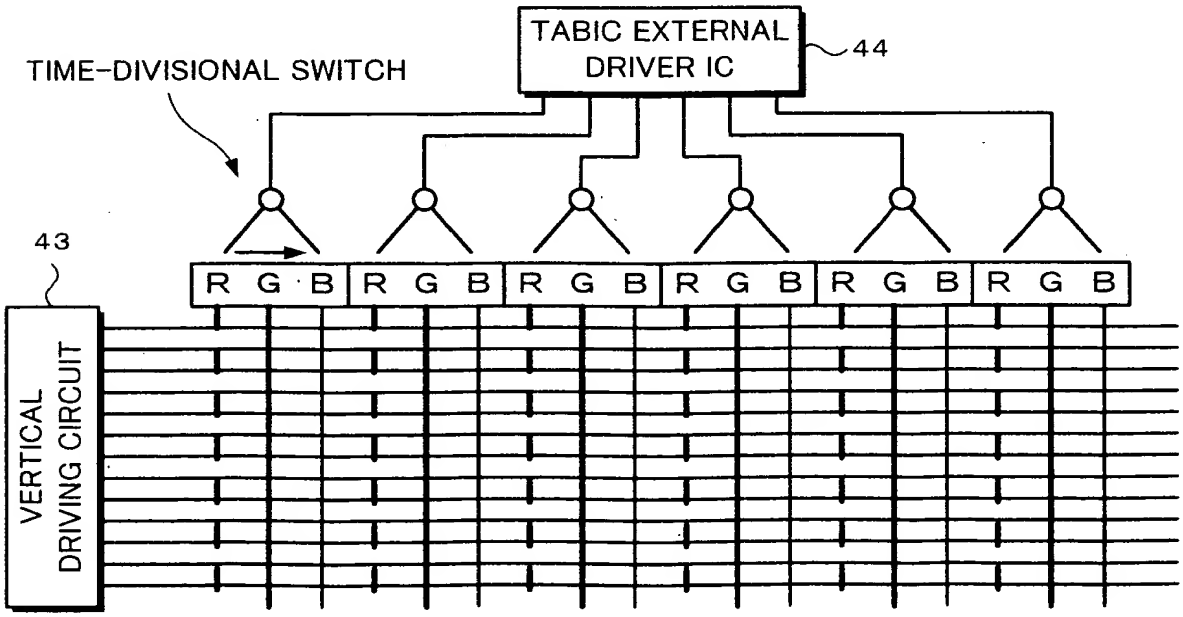


Fig. 14

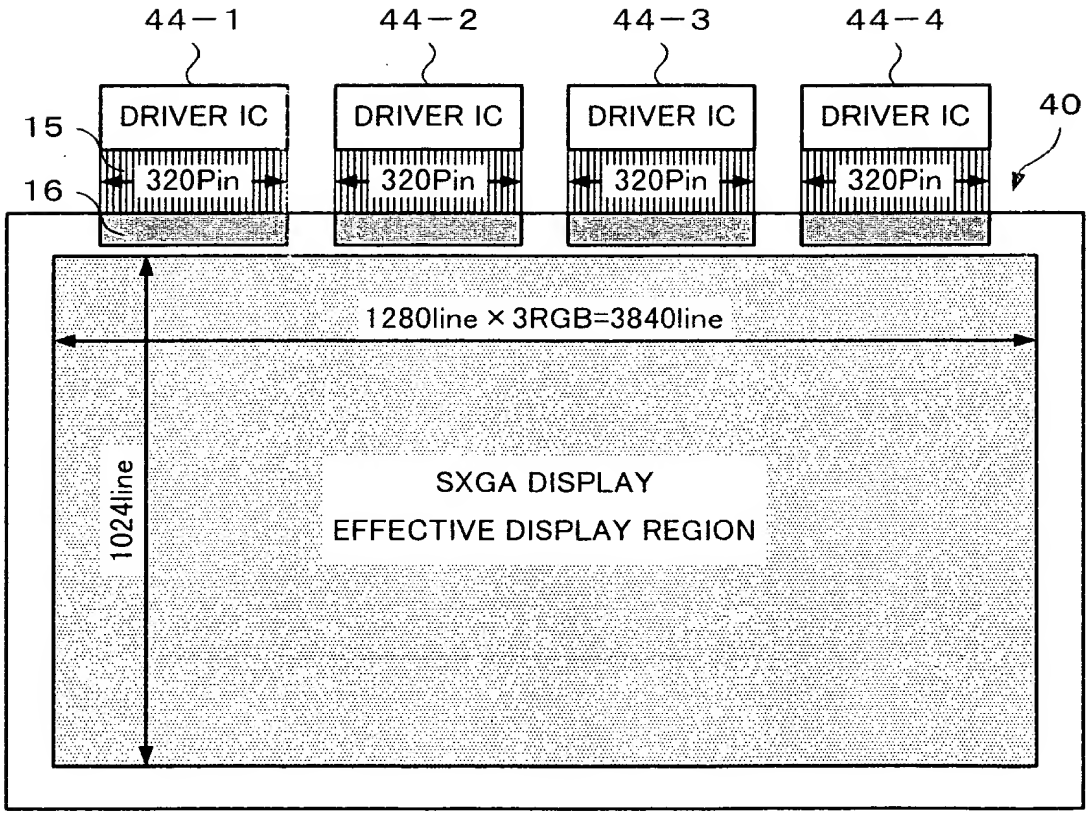

44−1
44−2
44−3
44−4
DRIVER IC
DRIVER IC
DRIVER IC
DRIVER IC
15
16
320Pin
320Pin
320Pin
320Pin
40
1280line × 3RGB=3840line
1024line
SXGA DISPLAY
EFFECTIVE DISPLAY REGION

Fig. 15

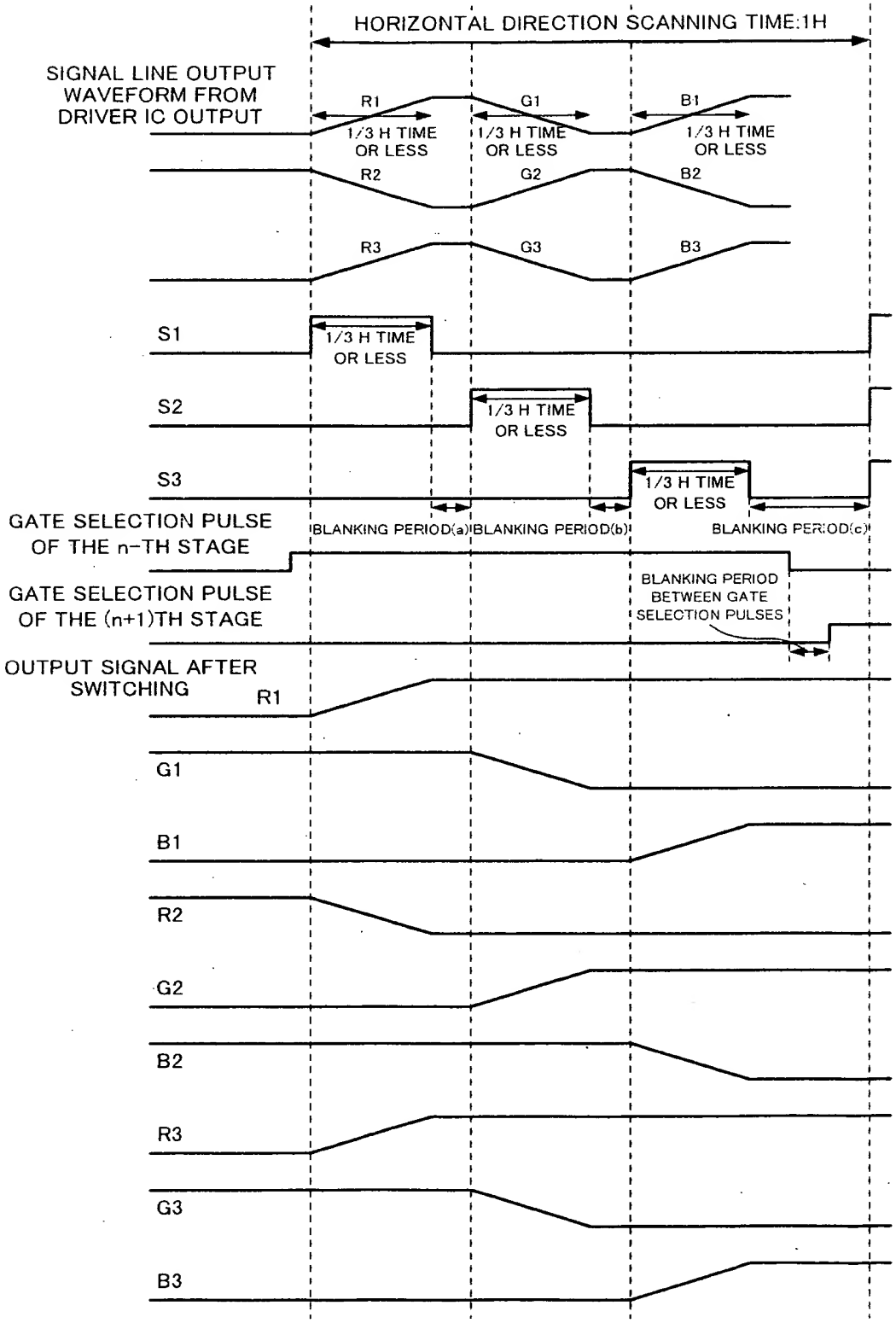

HORIZONTAL DIRECTION SCANNING TIME:1H
SIGNAL LINE OUTPUT WAVEFORM FROM DRIVER IC OUTPUT
R1
G1
B1
1/3 H TIME OR LESS
1/3 H TIME OR LESS
1/3 H TIME OR LESS
R2
G2
B2
R3
G3
B3
S1
1/3 H TIME OR LESS
S2
1/3 H TIME OR LESS
S3
1/3 H TIME OR LESS
BLANKING PERIOD(a)
BLANKING PERIOD(b)
BLANKING PERIOD(c)
GATE SELECTION PULSE OF THE n-TH STAGE
GATE SELECTION PULSE OF THE (n+1)TH STAGE
BLANKING PERIOD BETWEEN GATE SELECTION PULSES
OUTPUT SIGNAL AFTER SWITCHING
R1
G1
B1
R2
G2
B2
R3
G3
B3

Fig. 16A

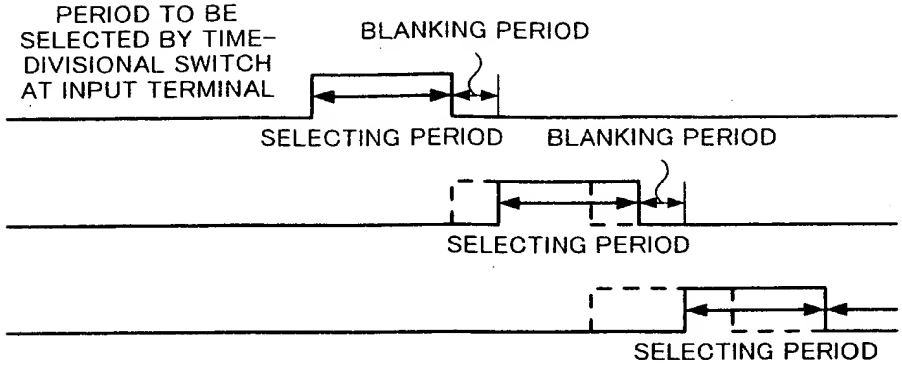


Fig. 16B

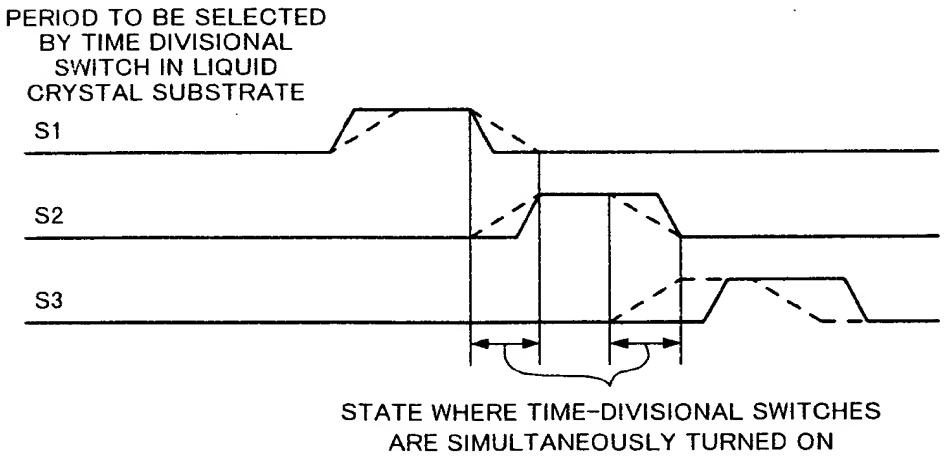


Fig. 16C

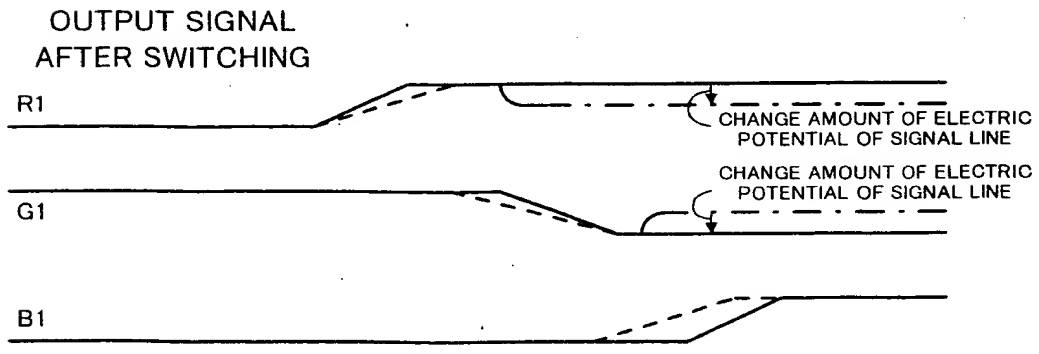


Fig. 17

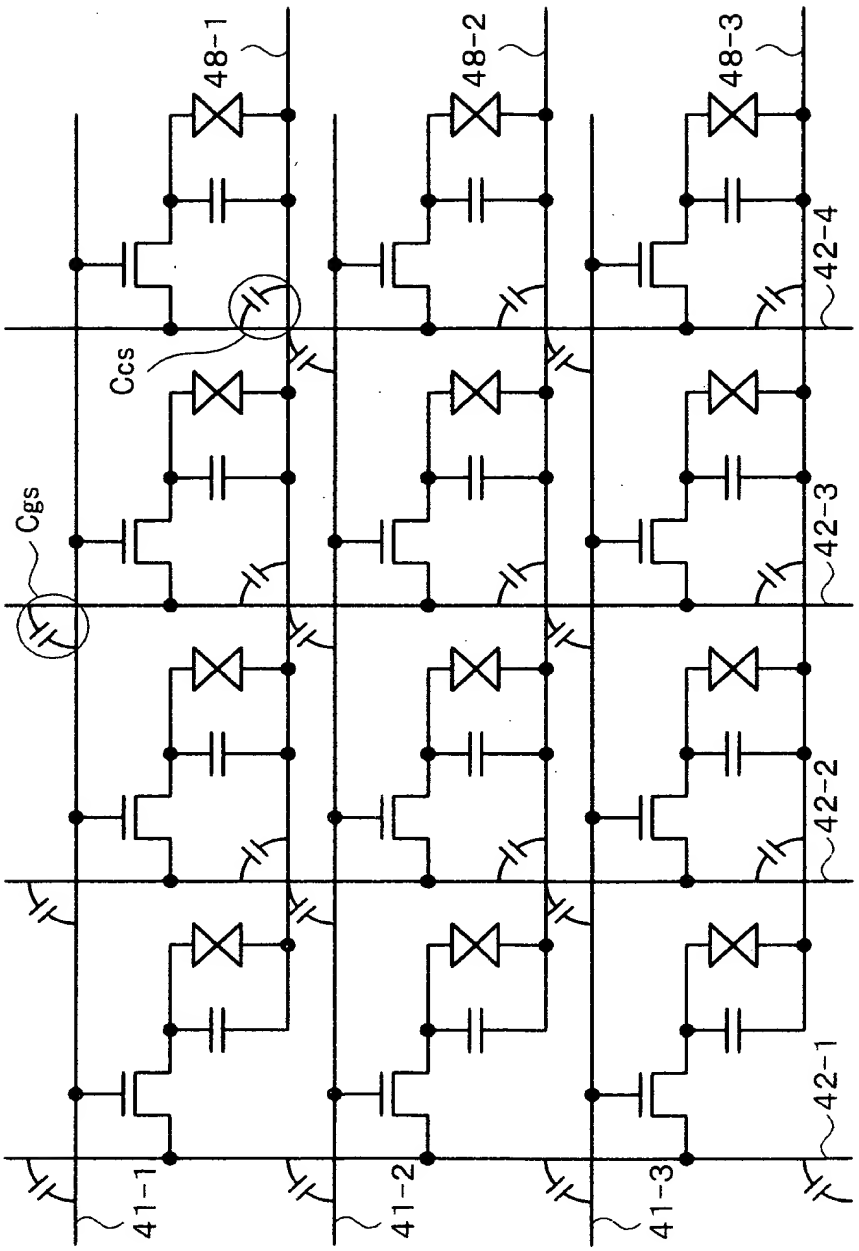


Fig. 18

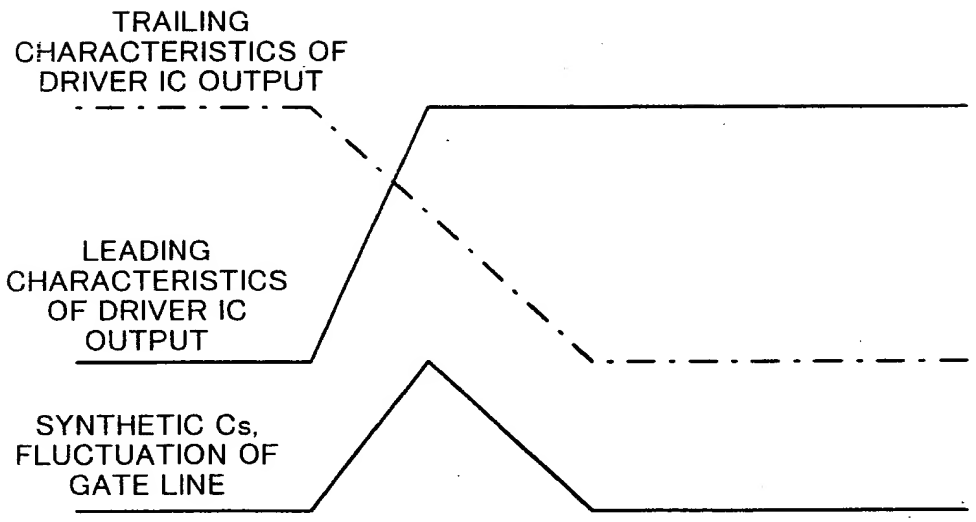

TRAILING CHARACTERISTICS OF DRIVER IC OUTPUT
LEADING CHARACTERISTICS OF DRIVER IC OUTPUT
SYNTHETIC Cs, FLUCTUATION OF GATE LINE

Fig. 19

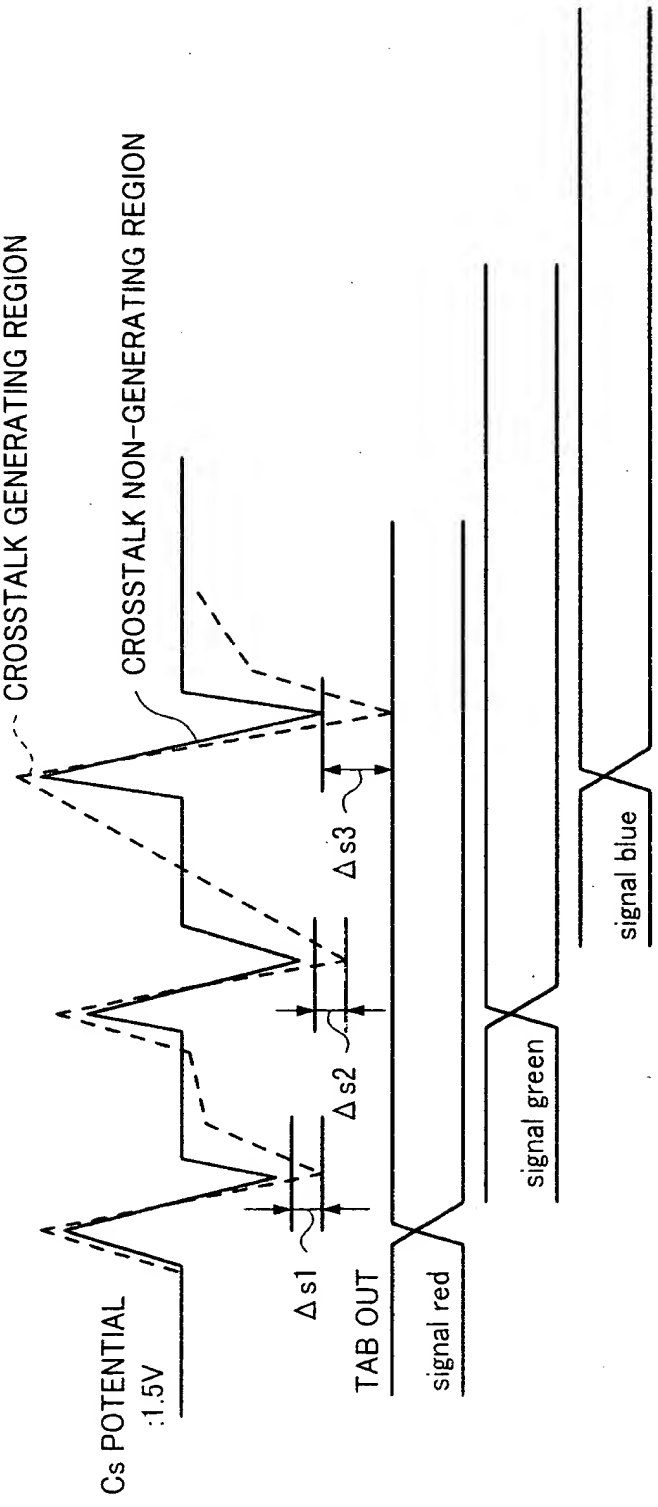

CROSSTALK GENERATING REGION
CROSSTALK NON-GENERATING REGION
Cs POTENTIAL
:1.5V
Δs1
Δs2
Δs3
TAB OUT
signal red
signal green
signal blue

Fig. 20

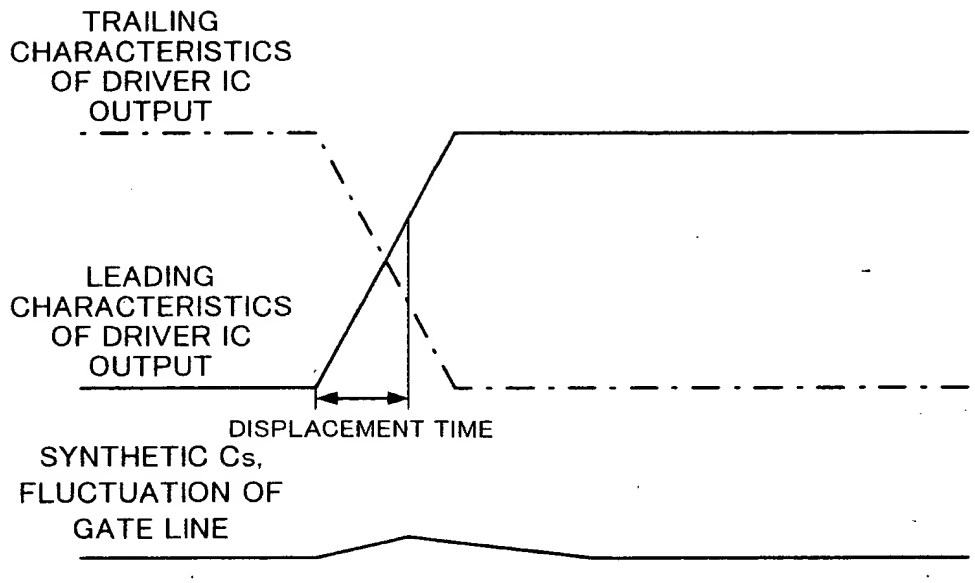

TRAILING CHARACTERISTICS OF DRIVER IC OUTPUT
LEADING CHARACTERISTICS OF DRIVER IC OUTPUT
DISPLACEMENT TIME
SYNTHETIC Cs, FLUCTUATION OF GATE LINE

Fig. 21

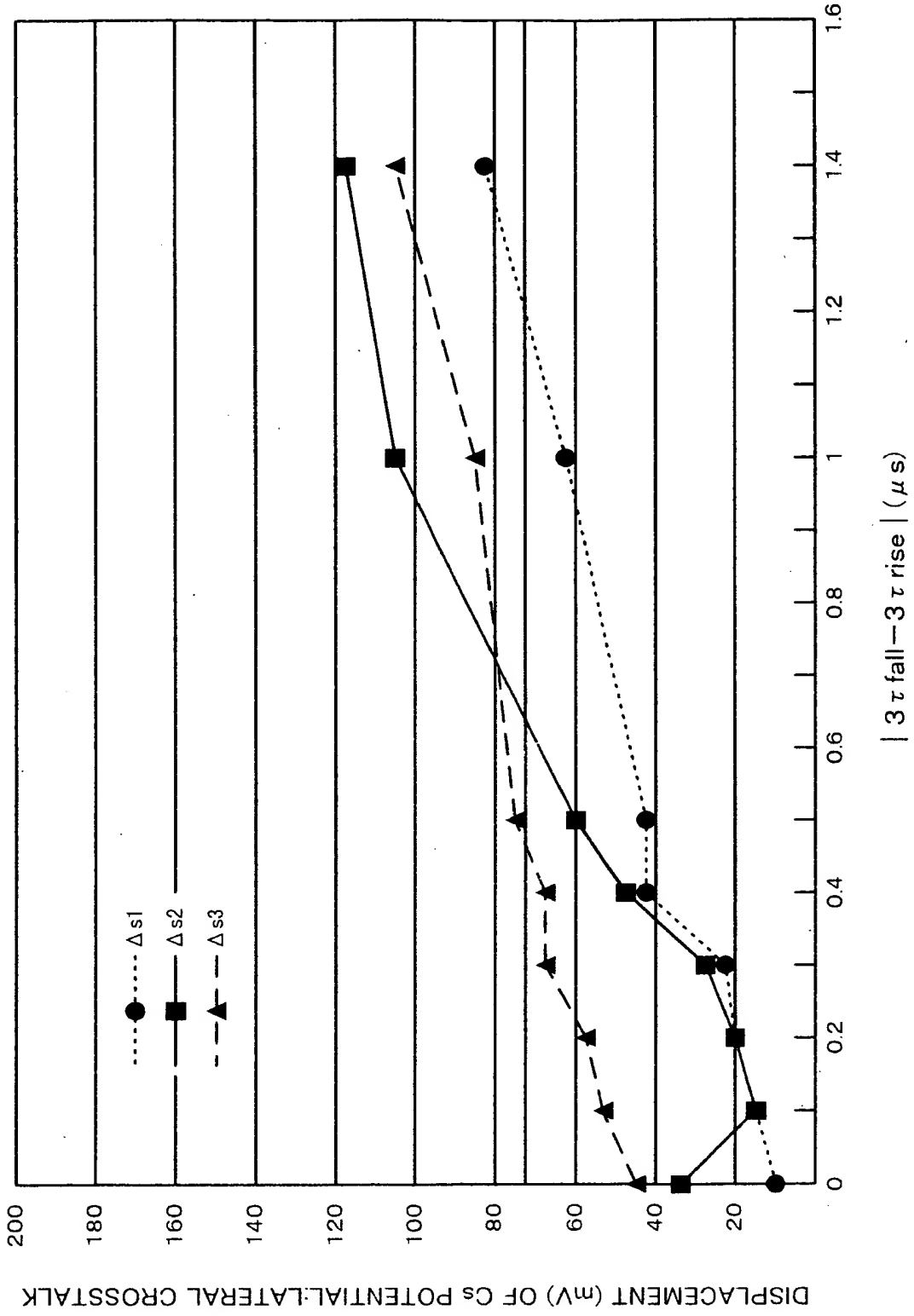

DISPLACEMENT (mV) OF Cs POTENTIAL LATERAL CROSSTALK
200
180
160
140
120
100
80
60
40
20
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
| 3τ fall − 3τ rise | (μs)
Δs1
Δs2
Δs3

Fig. 22

HORIZONTAL SCANNING TIME	21.537 μs	15.63 μs	12.504 μs	10.971 μs
TIME TO BE SELECTED BY TIME-DIVISIONAL SWITCH	3 μs	3 μs	3 μs	2 μs
THROUGHRATE BY EXTERNAL IC	2 μs	2 μs	2 μs	1.5 μs
BLANKING PERIOD	2 μs	1 μs	1 μs	1 μs
INVERSION DISPLAY METHOD	DOT INVERSION	DOT INVERSION	DOT INVERSION	DOT INVERSION
DOT FREQUENCY	78.75MHz	108MHz	135MHz	157.5MHz

Fig. 23

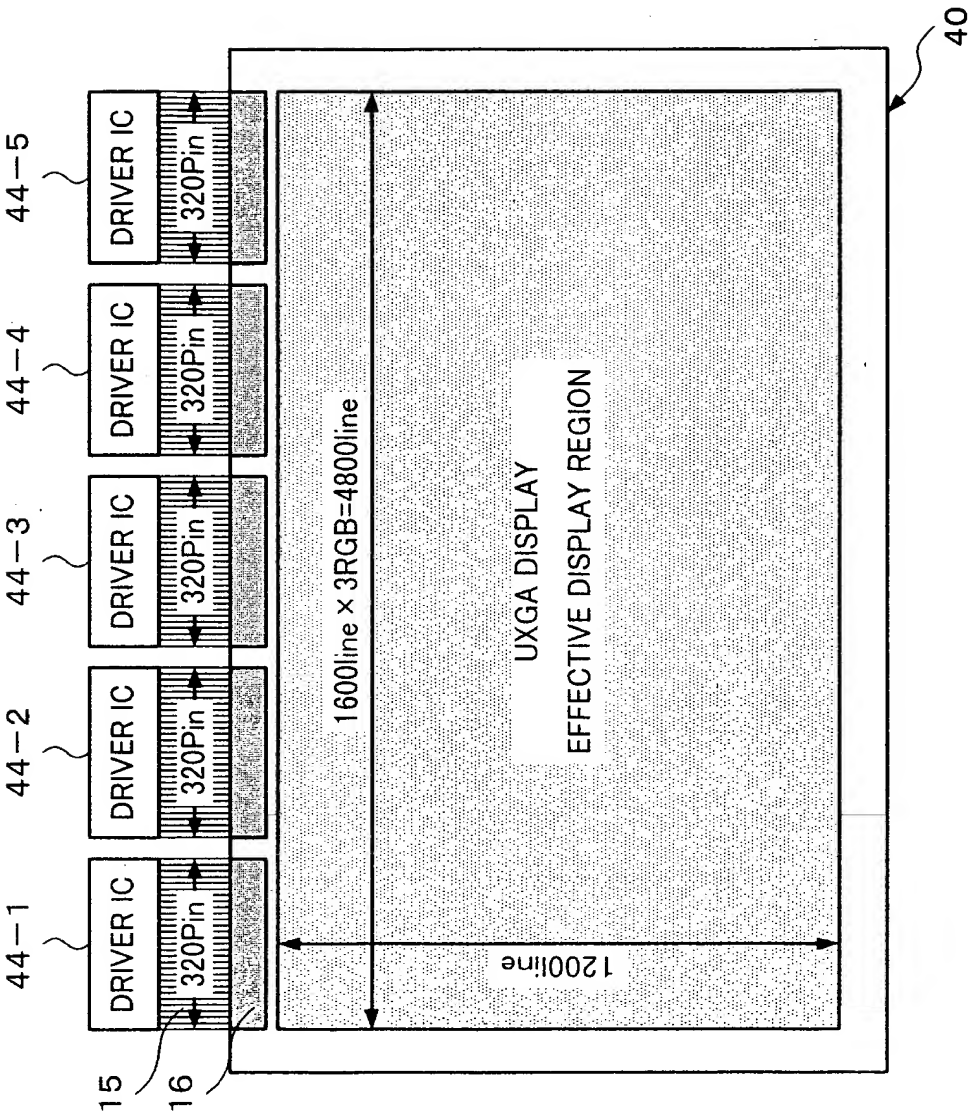

40
44-1
44-2
44-3
44-4
44-5
DRIVER IC
320Pin
15
16
1600line × 3RGB=4800line
1200line
UXGA DISPLAY
EFFECTIVE DISPLAY REGION

Fig. 24

HORIZONTAL SCANNING TIME	16 μs	13.333 μs	12.308 μs	11.429 μs	10.667 μs	10 μs	9.412 μs
TIME TO BE SELECTED BY TIME-DIVISIONAL SWITCH	3 μs	3 μs	3 μs	2.5 μs	2 μs	2 μs	2 μs
THROUGHRATE BY EXTERNAL IC	2 μs	2 μs	2 μs	2 μs	1.5 μs	1.5 μs	1.5 μs
BLANKING PERIOD	1 μs	1 μs	1 μs	1 μs	1 μs	1 μs	1 μs
INVERSION DISPLAY METHOD	DOT INVERSION	DOT INVERSION	DOT INVERSION	DOT INVERSION	DOT INVERSION	DOT INVERSION	DOT INVERSION
DOT FREQUENCY	135MHz	162MHz	175.5MHz	189MHz	202.5MHz	216MHz	229.5MHz

Fig. 25

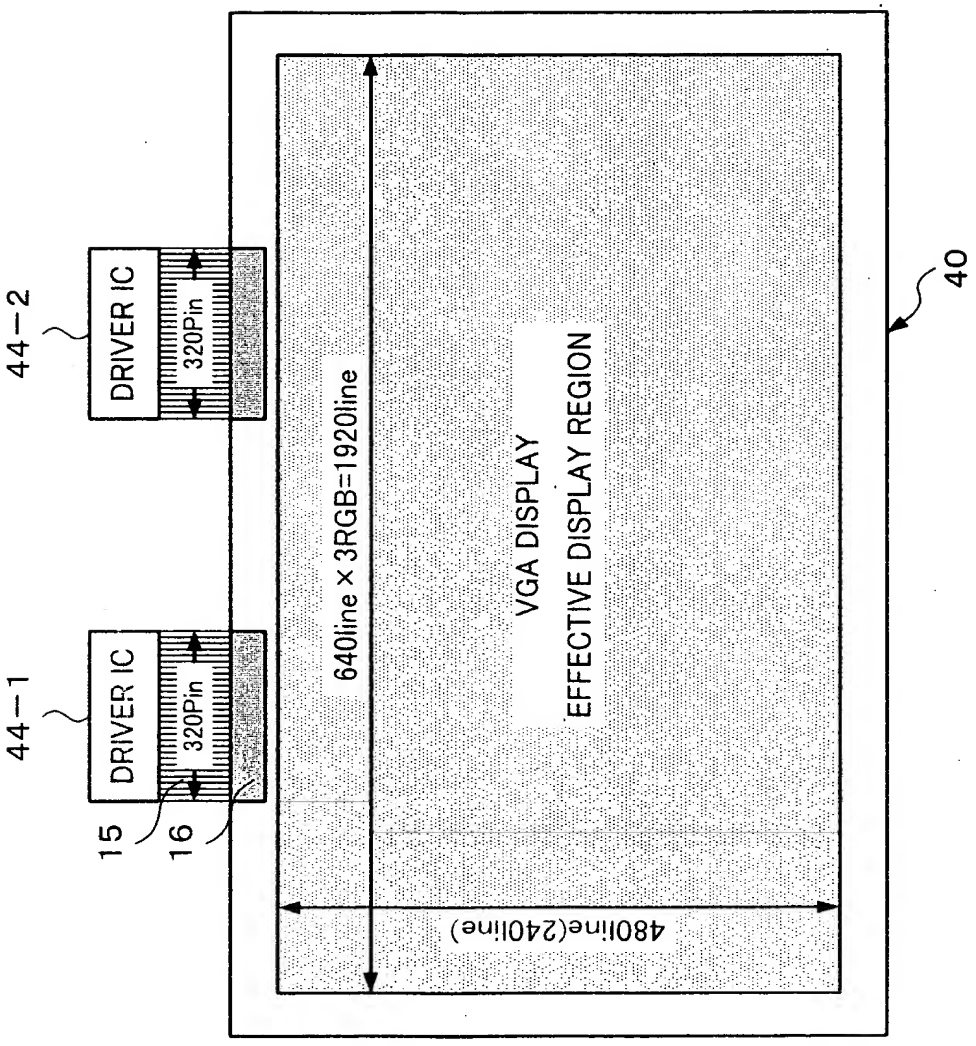

44-2
DRIVER IC
320Pin
44-1
DRIVER IC
320Pin
15
16
640line × 3RGB=1920line
480line(240line)
VGA DISPLAY
EFFECTIVE DISPLAY REGION
40

Fig. 26

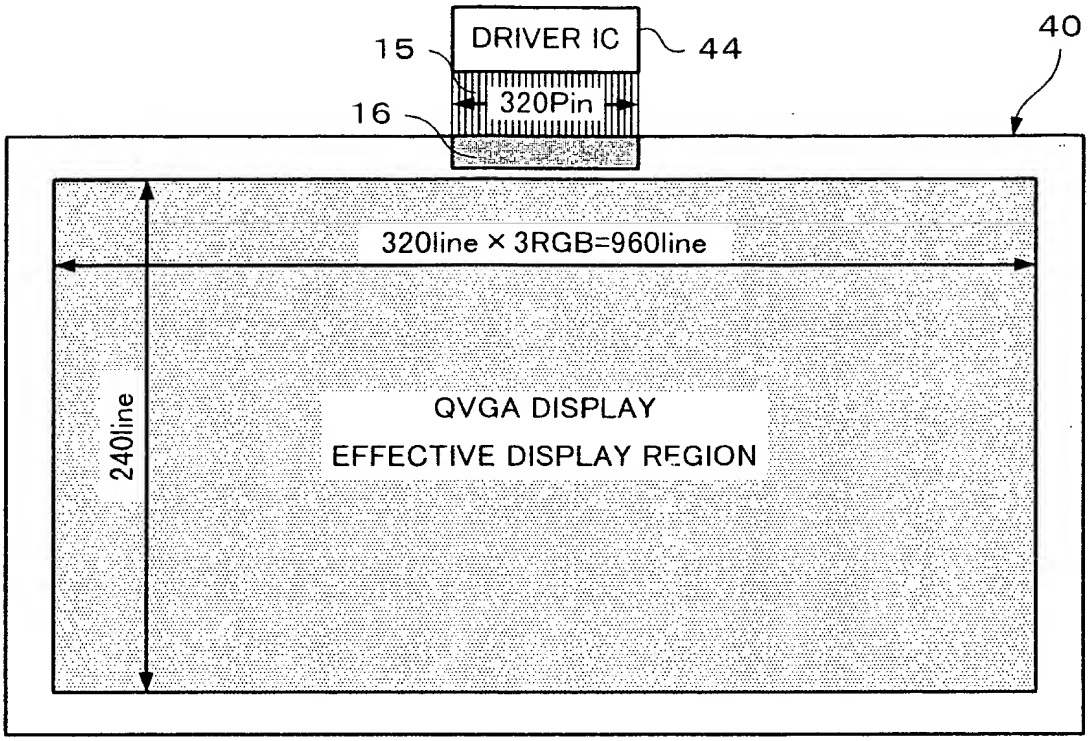


Fig. 27

	VGA	QVGA(1)	QVGA(2)
THE NUMBER OF PIXELS	HORIZONTAL:640 × 3RGB VERTICAL:480	HORIZONTAL:320 × 3RGB VERTICAL:240	HORIZONTAL:320 × 3RGB VERTICAL:240
HORIZONTAL SCANNING TIME	31.778 μs	63.492 μs	70.667 μs
TIME TO BE SELECTED BY TIME-DIVISIONAL SWITCH	6.774 μs	14.6 μs	10.0 μs
THROUGHRATE BY EXTERNAL IC	3 μs	3 μs	3 μs
BLANKING PERIOD	PERIOD(a),(b): 1.7 μs PERIOD(c): 8.056 μs	PERIOD(a),(b): 3 μs PERIOD(c): 13.692 μs	PERIOD(a),(b): 7 μs PERIOD(c): 26.667 μs
INVERSION DISPLAY METHOD	1H VCOM INVERSION	1H VCOM INVERSION	1H VCOM INVERSION

Fig. 28

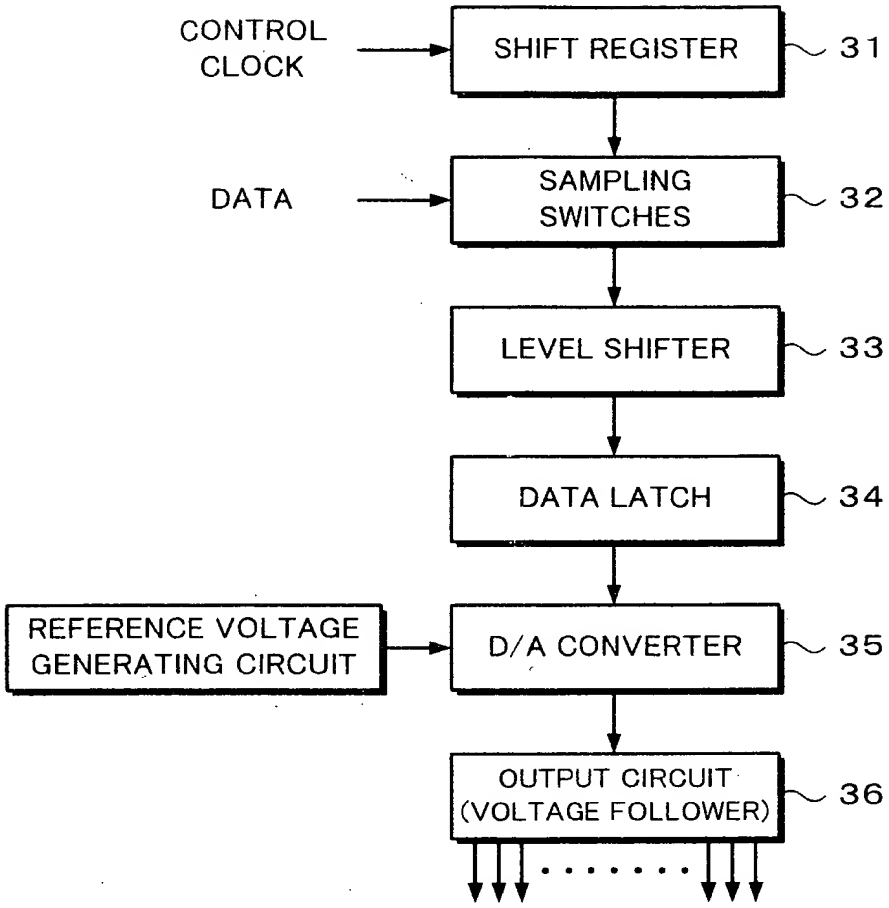

CONTROL
CLOCK
SHIFT REGISTER
31
DATA
SAMPLING
SWITCHES
32
LEVEL SHIFTER
33
DATA LATCH
34
REFERENCE VOLTAGE
GENERATING CIRCUIT
D/A CONVERTER
35
OUTPUT CIRCUIT
(VOLTAGE FOLLOWER)
36

Fig. 29

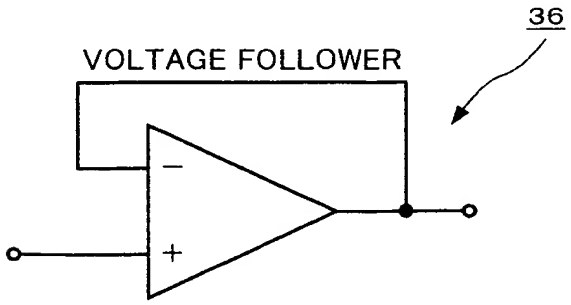

36
VOLTAGE FOLLOWER
−
+

Fig. 30

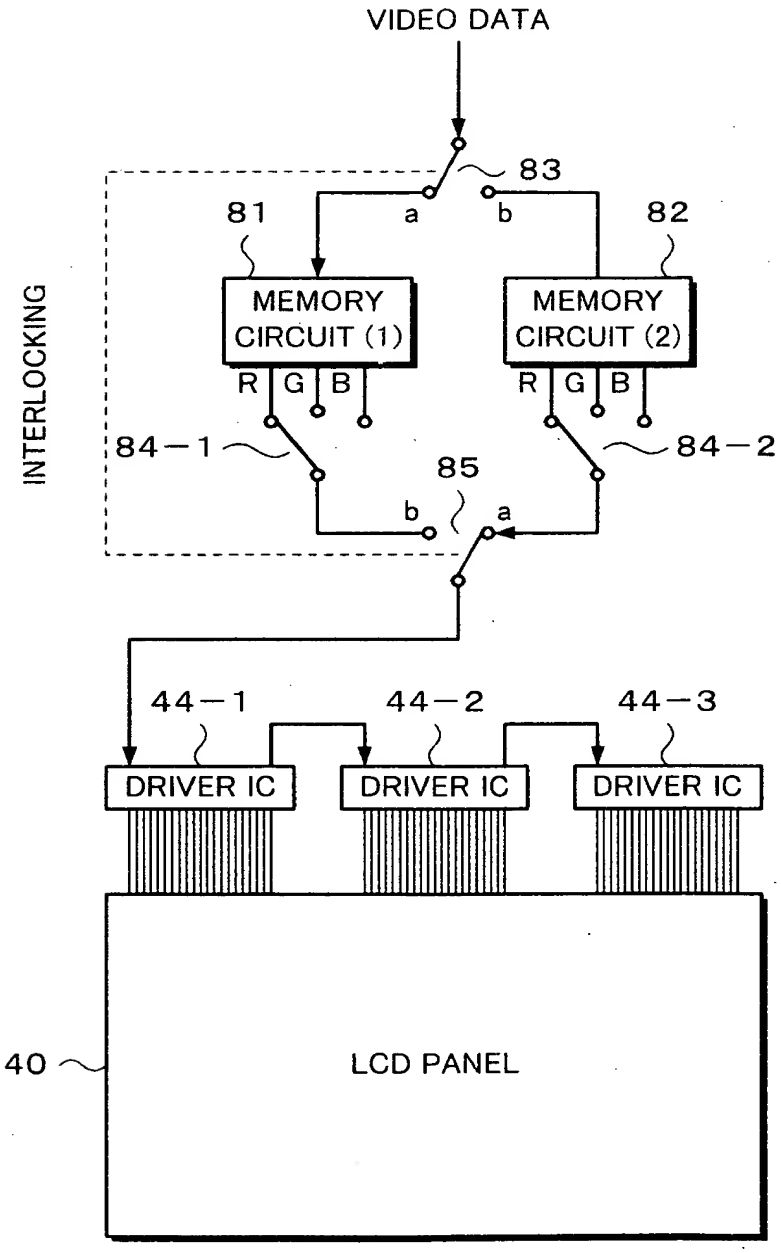

VIDEO DATA
83
a
b
81
82
MEMORY CIRCUIT (1)
MEMORY CIRCUIT (2)
R G B
R G B
INTERLOCKING
84−1
84−2
85
b
a
44−1
44−2
44−3
DRIVER IC
DRIVER IC
DRIVER IC
40
LCD PANEL

Fig. 31

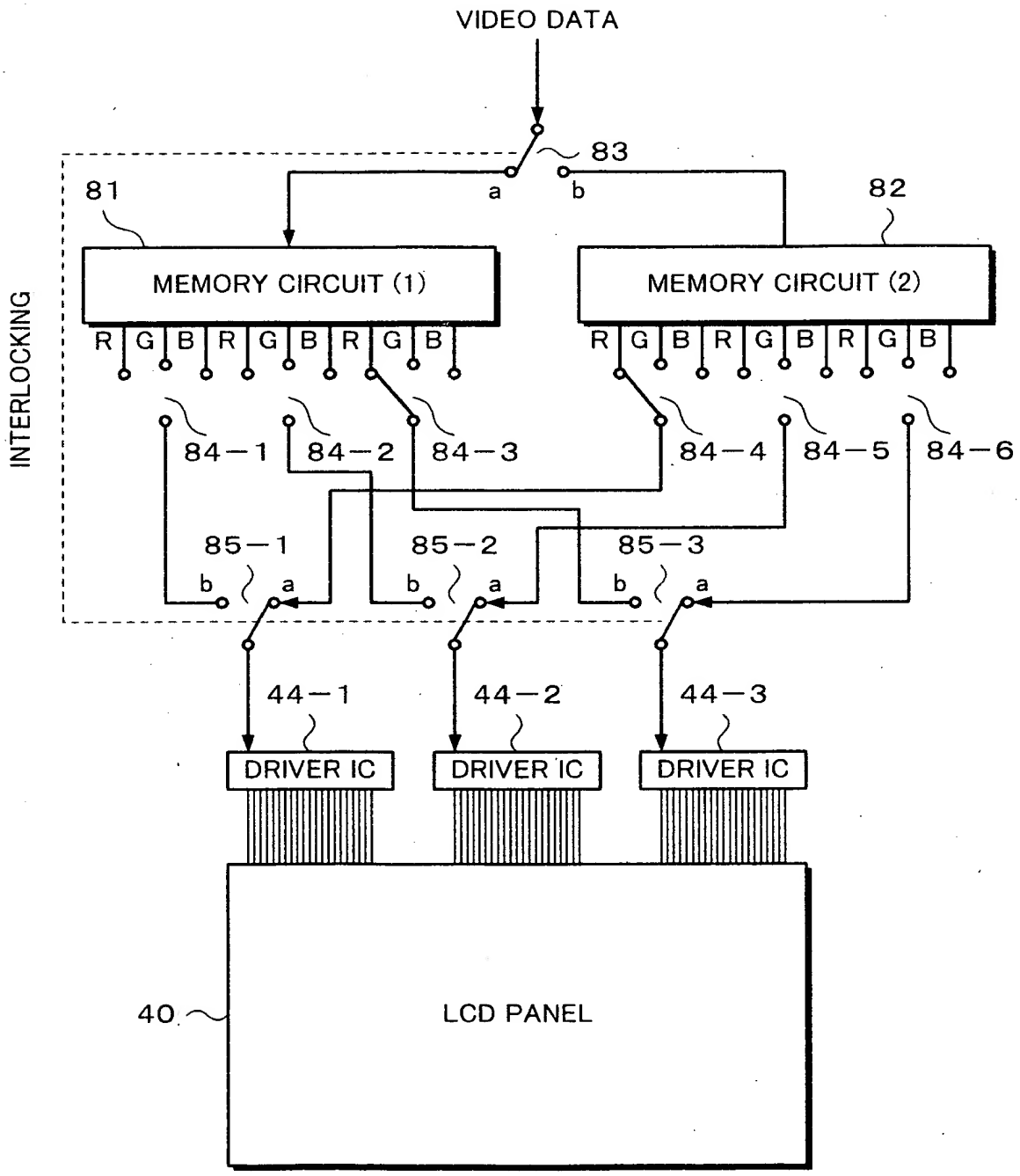

VIDEO DATA
83
a
b
81
82
INTERLOCKING
MEMORY CIRCUIT (1)
MEMORY CIRCUIT (2)
R G B R G B R G B
R G B R G B R G B
84−1
84−2
84−3
84−4
84−5
84−6
85−1
85−2
85−3
b
a
44−1
44−2
44−3
DRIVER IC
DRIVER IC
DRIVER IC
40
LCD PANEL

Fig. 32A

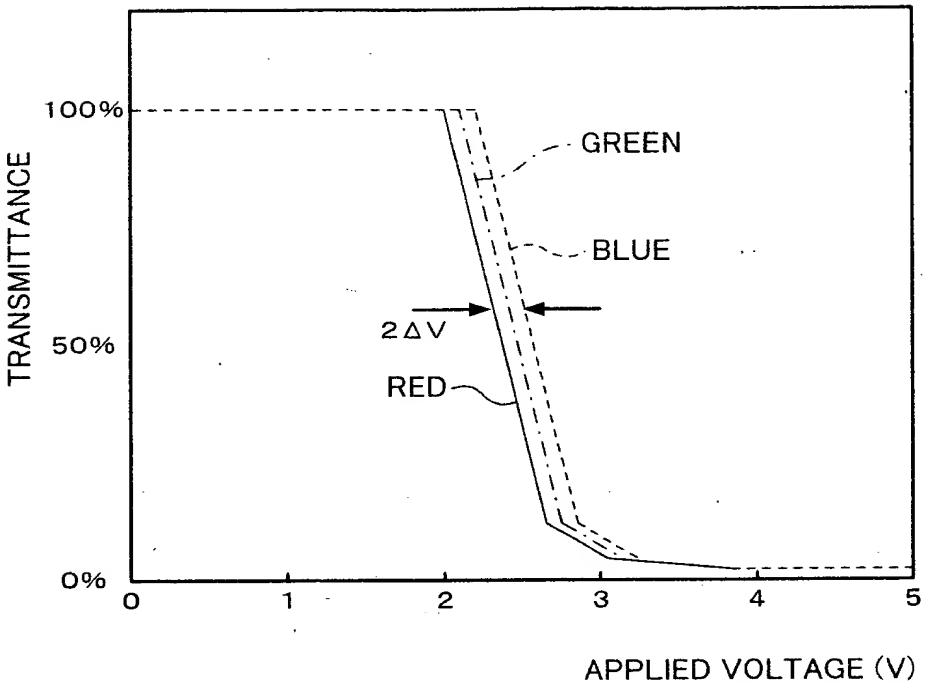


Fig. 32B

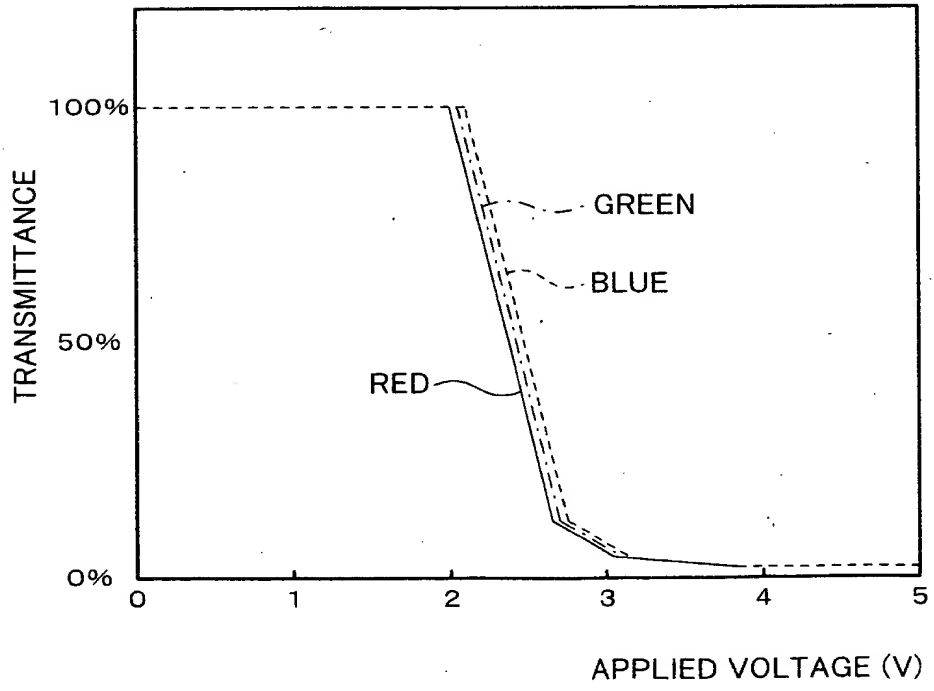


Fig. 33A

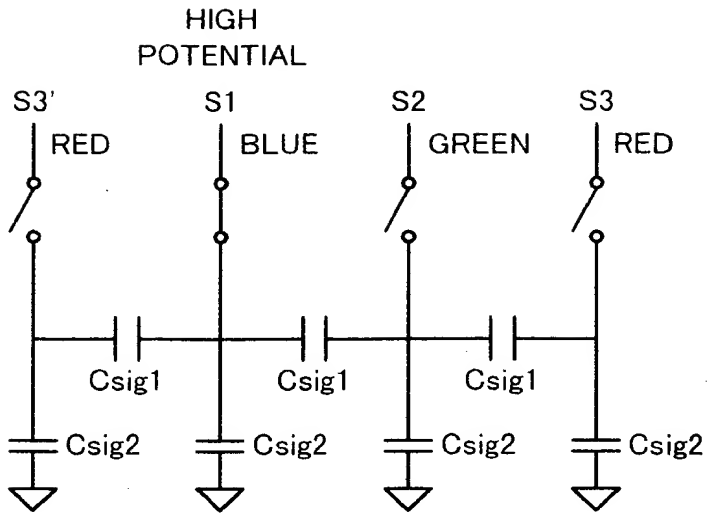


Fig. 33B

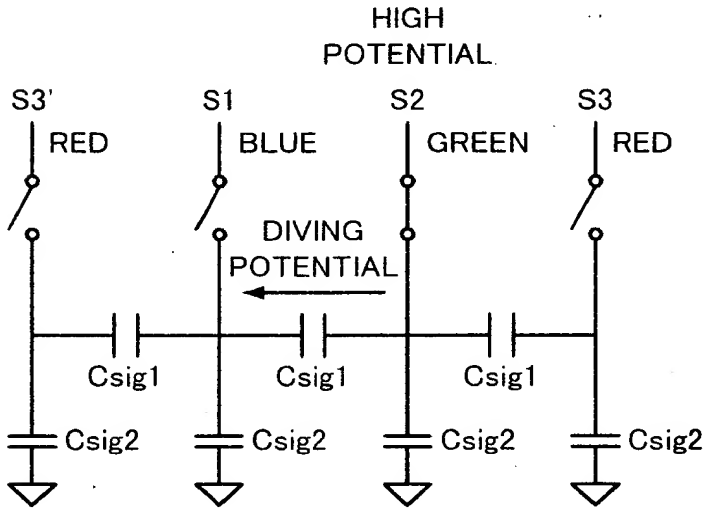


Fig. 33C

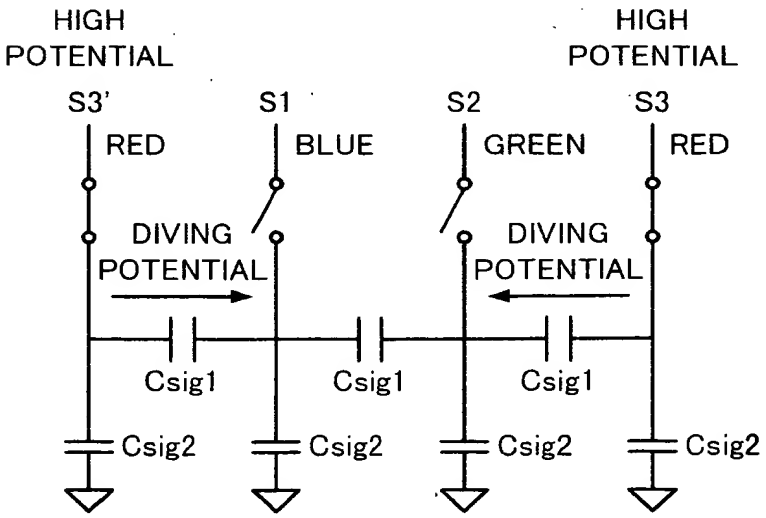


Fig. 34

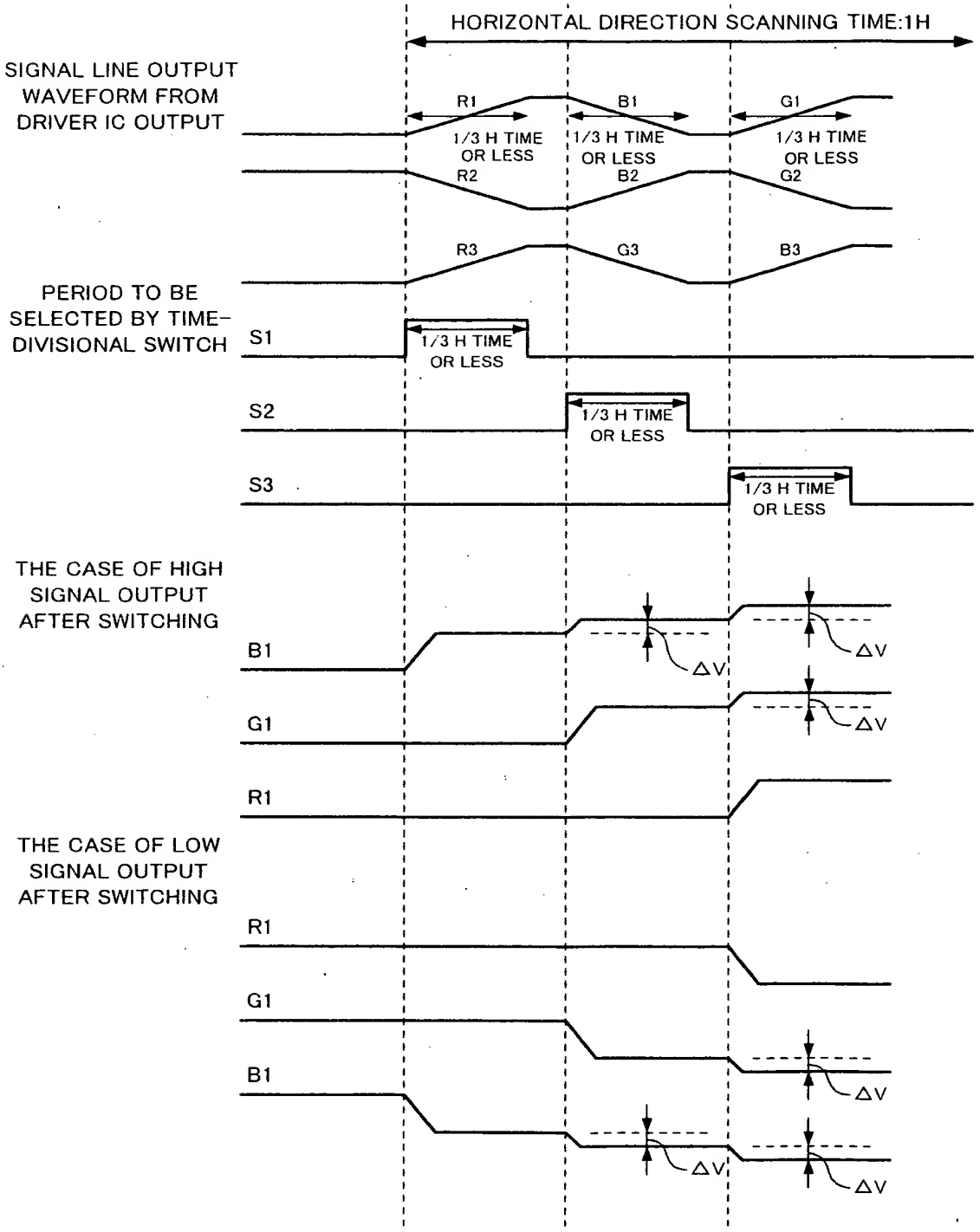

HORIZONTAL DIRECTION SCANNING TIME:1H
SIGNAL LINE OUTPUT WAVEFORM FROM DRIVER IC OUTPUT
R1
B1
G1
1/3 H TIME OR LESS
R2
B2
G2
R3
G3
B3
PERIOD TO BE SELECTED BY TIME-DIVISIONAL SWITCH
S1
S2
S3
THE CASE OF HIGH SIGNAL OUTPUT AFTER SWITCHING
ΔV
THE CASE OF LOW SIGNAL OUTPUT AFTER SWITCHING

Fig. 35A

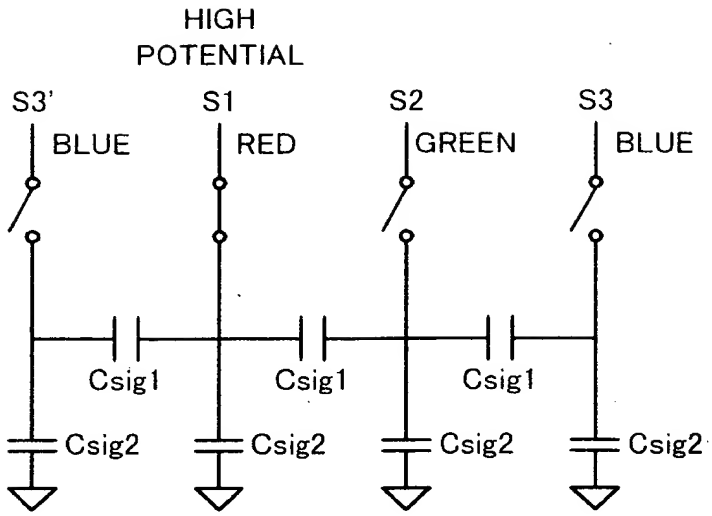


Fig. 35B

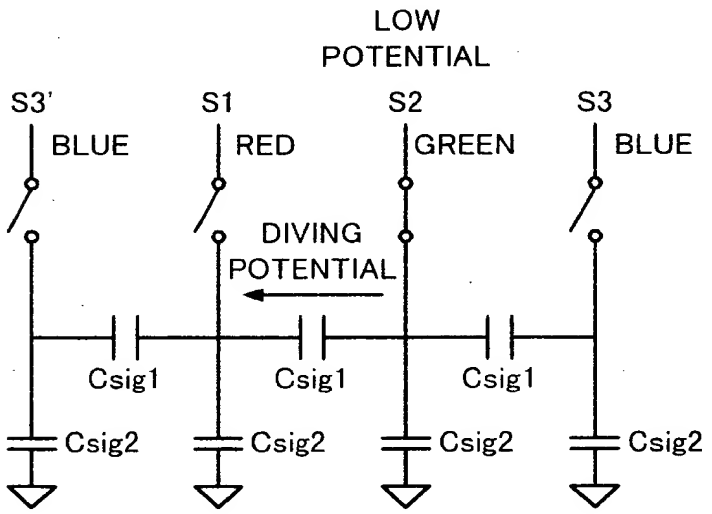


Fig. 35C

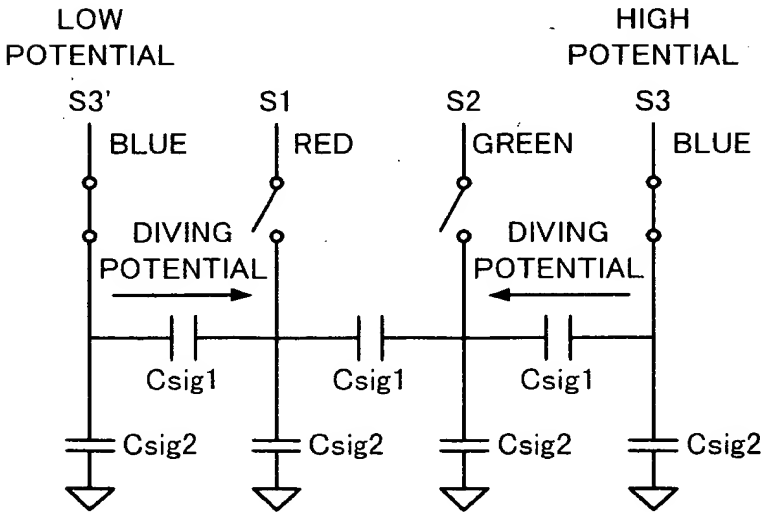


Fig. 36

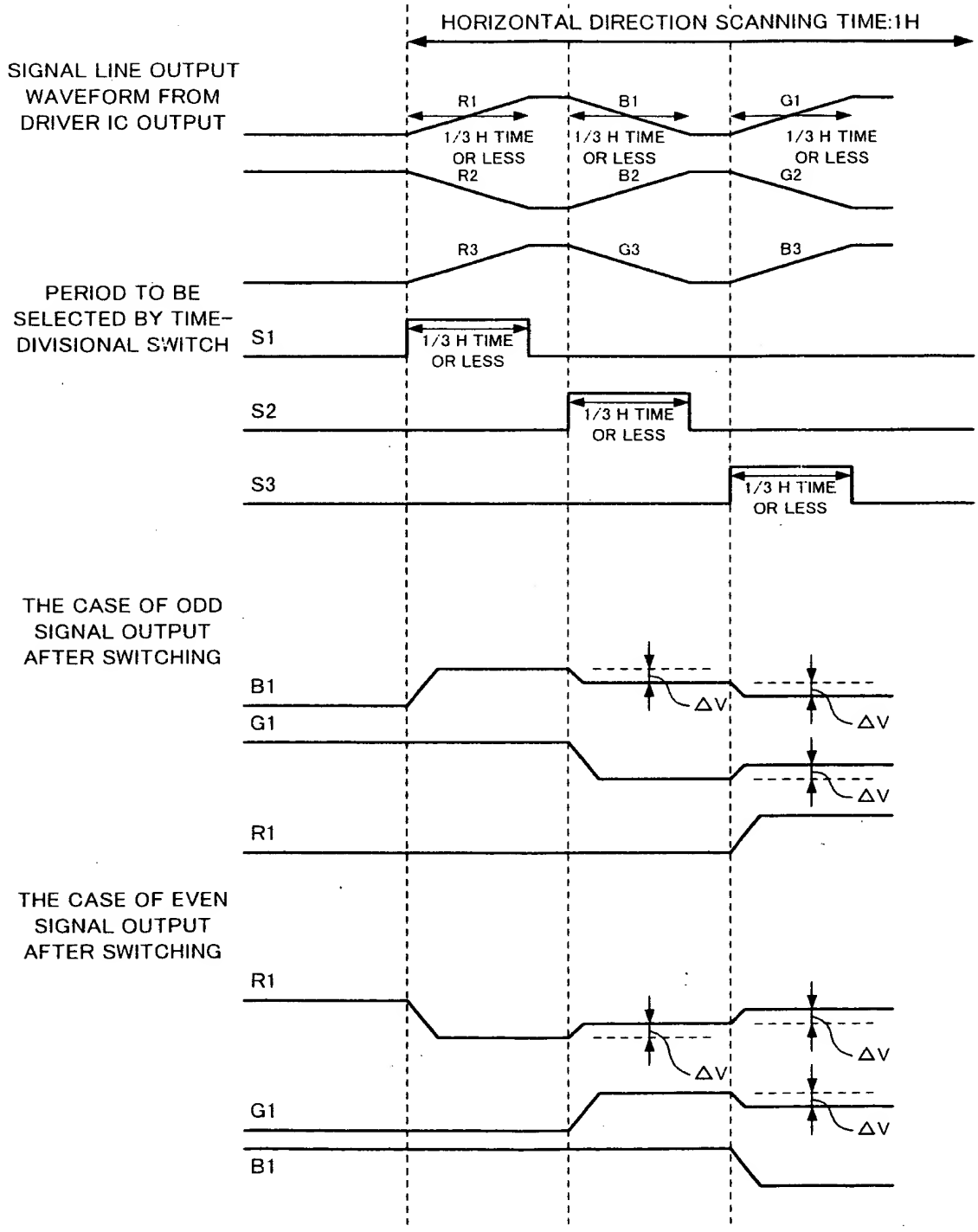
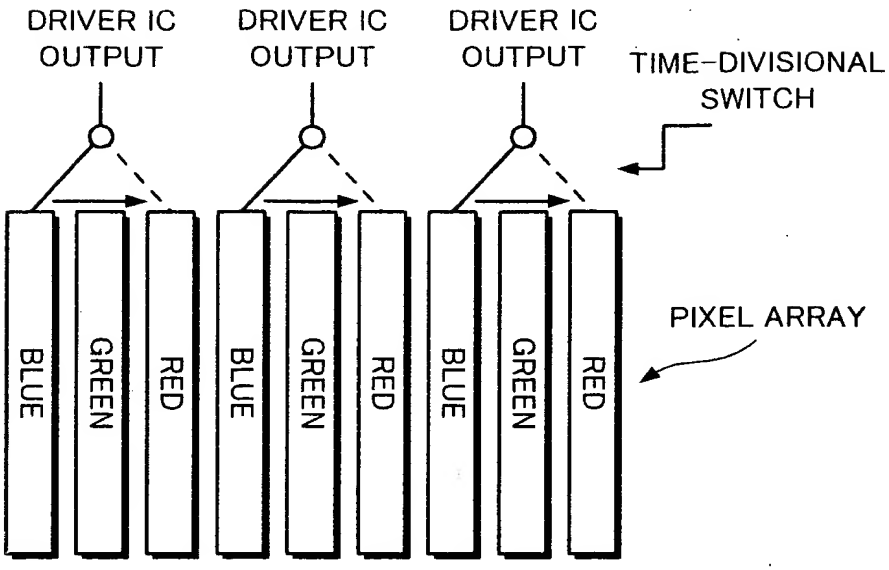
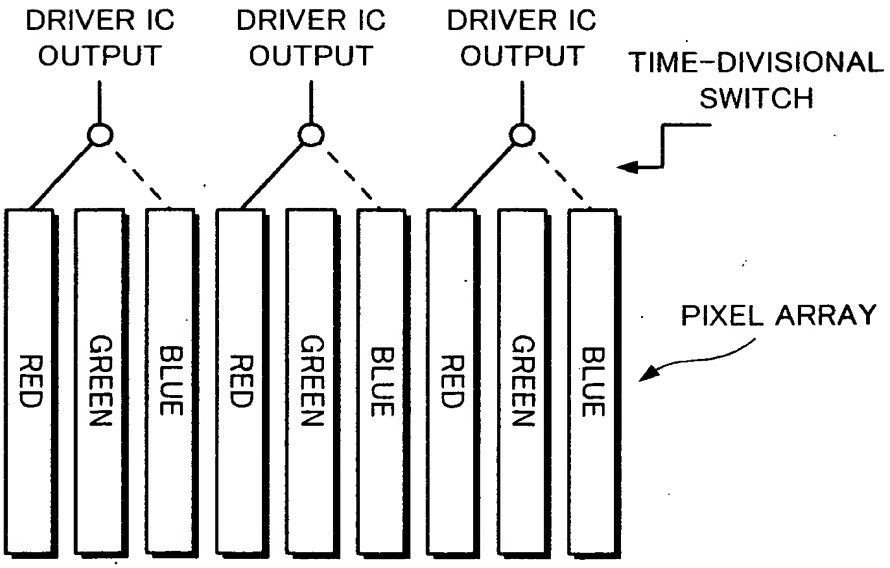

HORIZONTAL DIRECTION SCANNING TIME:1H
SIGNAL LINE OUTPUT WAVEFORM FROM DRIVER IC OUTPUT
R1
B1
G1
1/3 H TIME OR LESS
R2
B2
G2
R3
G3
B3
PERIOD TO BE SELECTED BY TIME-DIVISIONAL SWITCH
S1
S2
S3
THE CASE OF ODD SIGNAL OUTPUT AFTER SWITCHING
ΔV
THE CASE OF EVEN SIGNAL OUTPUT AFTER SWITCHING

Fig. 37A



1H INVERSION DRIVING METHOD

Fig. 37B



DOT INVERSION DRIVING METHOD

10, 40.. LIQUID CRYSTAL DISPLAY PANEL
11-1 ~ 11-3, 41-1 ~ 41-3.. GATE LINE
12-1 ~ 12-6, 42-1 ~ 42-6.. SIGNAL LINE
13, 43.. VERTICAL DRIVING CIRCUIT
14-1 ~ 14-3, 44-1 ~ 44-5.. DRIVER IC
20.. PIXEL
21.. THIN FILM TRANSISTOR
22.. ADDITIONAL CAPACITOR
23.. LIQUID CRYSTAL CAPACITOR
31.. HORIZONTAL SHIFT REGISTER
32.. SAMPLING SWITCHES
33.. LEVEL SHIFTER
34.. DATA LATCHES
35.. D/A CONVERTER (DIGITAL/ANALOG CONVERTING CIRCUIT)
36.. OUTPUT CIRCUIT
81, 82.. MEMORY CIRCUIT